A Review of Silicon Carbide Power Devices in Electric Vehicle Drive Systems

Yanbo Zhang*

College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing, 210016, China

*2912838957@qq.com

Abstract

Transportation electrification and high-voltage fast charging are driving traction inverters toward higher efficiency, greater power density and deeper integration. 4H-SiC, with its high critical electric field, high thermal conductivity and rapid switching capability, has emerged as a key device platform for 800-V-class electric drivetrains. We organize the application of SiC MOSFETs and Schottky barrier diodes in this review, covering material and device fundamentals through to drivetrain topologies, inverter control, packaging, thermal management, reliability and future trends. From the literature it emerges that SiC can lower switching loss, especially under light load and at elevated switching frequencies, and enables smaller passive and cooling elements. These benefits, however, are contingent on coordinated design of the dc-bus voltage, topology, modulation, gate drive, parasitics, thermal path and vehicle mission profile. Major barriers include the cost of substrates and epitaxy, gate-oxide stability, electromagnetic interference arising from high dv/dt, limited short-circuit withstand time and package fatigue under high heat flux. Future progress is anticipated from 200-mm manufacturing, advanced device structures, low-inductance double-sided cooling packages, heterogeneous SiC/GaN architectures and health-aware control. Rather than universally displacing silicon, SiC will deliver the greatest value where its device-level advantages can be converted into verifiable lifetime benefits at vehicle level.

Keywords

Silicon carbide, electric vehicle, electric drive, traction inverter, thermal management, reliability.

1. Introduction

Electric vehicles (EVs) have moved from demonstration applications into large-scale deployment, driven by the global energy transition and transportation decarbonization targets. The International Energy Agency reports that global EV sales continue to grow, and coordinated upgrades in battery packs, charging infrastructure and electric drive systems have become a focal point of industrial competition [1]. Within the vehicle energy chain, the traction inverter converts the dc power of the battery pack into the ac power required by the electric motor; its efficiency, volume, power density and thermal management directly affect driving range, dynamic performance and vehicle packaging. As the voltage platform evolves from the conventional 400 V to 800 V and beyond, the inverter must operate at higher bus voltages, across wider load ranges and under more compact cooling conditions. Traditional Si IGBTs are limited by their material critical breakdown field, switching tail current and high-temperature performance, so that problems with high-frequency losses and system volume become increasingly prominent.

Among the polytypes of silicon carbide, a representative wide-bandgap semiconductor, 4H-SiC combines a wide bandgap, a high critical breakdown field, high thermal conductivity and a high carrier saturation velocity. Relative to Si devices, SiC devices at the same blocking voltage can use a thinner drift region with higher doping concentration, thereby reducing the specific on-resistance; the majority-carrier conduction mechanism also allows SiC MOSFETs to avoid the significant tail current observed during IGBT turn-off [2,3]. SiC Schottky barrier diodes exhibit nearly negligible minority-carrier storage, which lowers the reverse-recovery loss in freewheeling paths. SiC MOSFETs and SiC SBDs have consequently been adopted progressively in traction inverters, onboard chargers and high-voltage dc–dc converters, and have become an important technology pathway for high-voltage EV power electronics [4].

Research in this area has expanded from device characteristics to vehicle-level applications. At the device level, the focus is on trench-gate structures, gate-oxide reliability, short-circuit robustness and avalanche robustness; at the inverter level, the emphasis is on two-level and multilevel topologies, loss modeling, modulation and switching-frequency optimization; at the module level, work concentrates on low-inductance packaging, silver sintering, double-sided cooling and power-cycling lifetime [5–9]. The advantages of SiC in switching loss and high-temperature operation are generally acknowledged in the literature, but the bus voltages, power ratings, switching frequencies, junction temperatures and operating conditions used across studies vary considerably, making quantitative device-to-device or system-to-system comparisons difficult without a unified benchmark. Furthermore, increasing switching speed reduces per-event switching energy but can exacerbate voltage overshoot, common-mode current and motor insulation stress; shrinking chip area lowers cost but may degrade short-circuit withstand capability and raise the density of heat flux per unit area.

The application of SiC in electric drive systems should therefore not be reduced to a direct drop-in replacement of Si IGBTs. Instead, an analysis chain from material properties, through device behavior, topology and control, to packaging, thermal management and vehicle-level benefits should be established. Taking 4H-SiC MOSFETs and SiC SBDs as primary subjects, we first introduce material and device fundamentals, then discuss the compatibility of different drivetrain topologies with SiC, inverter control and switching-frequency trade-offs, packaging, thermal management and reliability issues, and finally identify bottlenecks in four areas (cost, gate oxide, EMI and short-circuit protection) and offer forward-looking assessments. The aim is to give a systematic reference for device selection and multi-physics co-design of EV electric drive systems.

In terms of methodology, we focus on recent publications in IEEE, IET and Chinese core journals, while retaining representative studies that elucidate material physics, device mechanisms and early system comparisons. The literature is not listed chronologically but is categorized by device, topology, control, packaging and vehicle levels, with particular attention to the boundary conditions that explain discrepancies among different research conclusions. For metrics such as efficiency, power density and cost that are easily influenced by prototype parameters, we do not extrapolate values from a single case to all vehicle platforms but instead analyze trends as functions of bus voltage, switching frequency, cooling conditions and mission profile. This organizational approach helps distinguish the intrinsic material advantages of SiC, problems solvable through engineering optimization and reliability risks that still require long-term data validation.

2. SiC Materials and Power Device Fundamentals

2.1. Properties of 4H-SiC

The conduction loss, blocking capability and high-temperature limits of a power semiconductor are first constrained by material properties. The bandgap of 4H-SiC is approximately three

times that of Si, and its critical breakdown field is roughly 8 to 10 times higher; high-voltage devices can therefore thin the drift region significantly and increase the doping concentration. In the Baliga figure of merit the critical breakdown field enters the theoretical evaluation of unipolar power devices to the third power, so SiC possesses a pronounced specific on-resistance advantage in the medium-to-high voltage range [3]. At the same time, the higher thermal conductivity facilitates heat transfer from the chip to the substrate and coolant, yet this does not imply that thermal design at the module level can be neglected, because a smaller SiC chip may in fact increase the heat flux per unit area. Table 1 lists the key material parameters, and Figure 1 illustrates the chain by which these material advantages propagate to electric drive system benefits.

Table 1. Comparison of typical material parameters between Si and 4H-SiC

Parameter	Si	4H-SiC	Implication for drive applications
Bandgap Eg (eV)	1.12	3.26	Lower high-temperature leakage; enhanced high-temperature capability
Critical field Ec (MV/cm)	≈0.3	≈2.5–3.0	Thinner drift region at the same blocking voltage; lower on-resistance
Thermal conductivity (W/(cm·K))	≈1.5	≈3.7–4.9	Facilitates heat transfer from chip to package
Electron mobility ($cm^2/(V·s)$)	≈1400	≈900	SiC channel mobility limited by interface states
Saturated drift velocity ($\times 10^7$ cm/s)	≈1.0	≈2.0	Supports faster switching transients
Relative dielectric constant	≈11.8	≈9.7	Affects junction capacitance and electric-field distribution

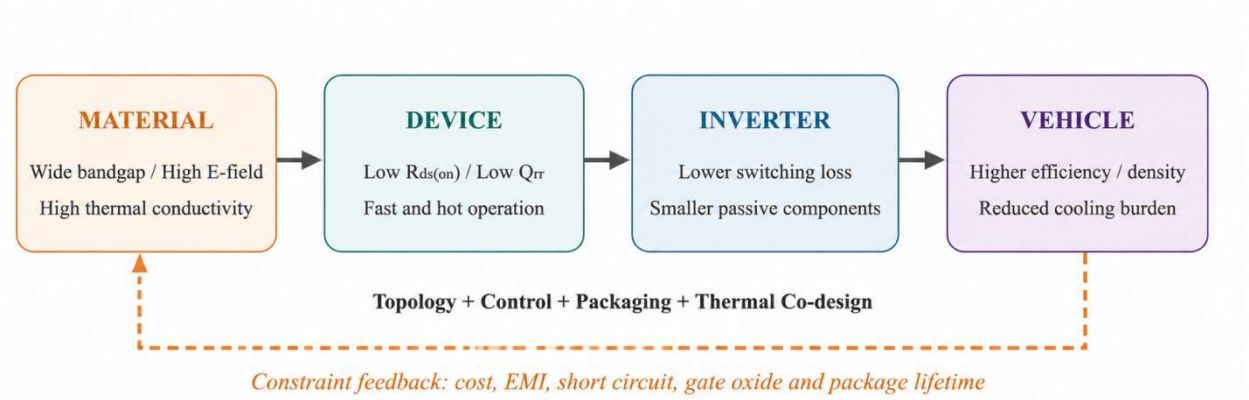

Figure 1. Chain by which SiC material advantages propagate to electric drive system benefits

2.2. Operating Characteristics of SiC SBDs and MOSFETs

Using a metal-semiconductor Schottky junction and conducting predominantly through majority carriers, the SiC SBD eliminates the significant minority-carrier storage process inherent in Si PiN diodes. Its reverse-recovery current arises mainly from junction-capacitance charging and discharging, and this reduces the additional losses incurred when the freewheeling diode turns off and the complementary switch turns on. Early drive and charging systems often used the 'Si IGBT + SiC SBD' hybrid approach to gain reverse-recovery improvement at relatively low retrofit cost; as SiC MOSFET costs have declined, the full-SiC half-bridge has gradually become the dominant implementation for high-voltage traction drives [2].

Two structural categories are generally distinguished for SiC MOSFETs: planar-gate and trench-gate. Planar-gate devices offer mature processing and relatively better short-circuit robustness, but the JFET-region resistance is larger; trench-gate designs increase channel density and

reduce on-resistance, yet impose stricter requirements on gate-oxide field distribution and manufacturing uniformity. The on-resistance of the device is composed of contributions from the channel, the JFET region, the drift region, the substrate and the contact resistance, all of which increase with rising junction temperature. Third-quadrant conduction may be handled by the MOS channel or by the body diode. To suppress bipolar degradation and reduce the reverse voltage drop, practical inverters typically prioritize MOS-channel conduction using appropriate dead-time and synchronous-rectification strategies.

2.3. High-Temperature, High-Frequency, and Loss Boundaries

Inverter semiconductor losses can be approximately decomposed into conduction losses and switching losses. MOSFET conduction loss is mainly related to the rms current and $R_{DS(on)}$, while the average switching loss can be written as $P_{sw} \approx f_s(E_{on} + E_{off})$, where f_s is the switching frequency and E_{on} and E_{off} are the turn-on and turn-off energy per event. SiC MOSFETs lack the significant tail current of IGBTs and possess smaller gate charge and output capacitance; under the same voltage and current conditions they generally exhibit lower switching energy, and the advantage becomes more pronounced as the switching frequency increases [5,10]. A higher frequency can reduce current ripple and filter volume and improve motor-control bandwidth, but device output-capacitance loss, gate-drive loss and high-frequency magnetic-component loss still grow; the system operating point therefore cannot be determined solely from the frequency that the device permits.

Temperature affects device performance in two ways. The wide bandgap of SiC reduces high-temperature leakage and permits higher junction-temperature designs; however, increasing $R_{DS(on)}$ with temperature raises conduction loss, and gate-oxide trap capture and emission cause threshold-voltage drift. In multi-chip parallel configurations the positive temperature coefficient aids steady-state current sharing, but switching transients are still influenced by differences in threshold voltage, inductance and drive-loop characteristics. High-temperature capability should therefore be understood as expanding the design margin rather than permitting long-term operation near the limiting junction temperature.

2.4. Key Constraints in Device Application

At the SiC/SiO_2 interface the density of interface states is higher than at the mature Si/SiO_2 interface, and this constitutes the primary limitation on channel mobility and gate stability. Long-term positive and negative gate-bias stress at elevated temperatures can induce threshold-voltage drift, and trench structures additionally require control of the electric field at the gate bottom. On the other hand, SiC chips are relatively small and exhibit high short-circuit current density; during a short circuit the junction temperature can rise rapidly within a few microseconds, leaving detection and turn-off circuitry very little time [7]. High-speed device switching also amplifies the effects of package and busbar parasitic inductance, causing voltage overshoot, ringing and spurious turn-on. It follows that the material figure of merit of SiC can be stably converted into electric drive system benefits only through the joint action of device structure, gate drive, low-parasitic packaging and protection strategies.

Comparing only rated voltage and room-temperature on-resistance should also be avoided in device selection. Datasheet switching energies are closely tied to the inductance of the test loop, gate resistance, bus voltage and load current; values from different manufacturers cannot be directly ranked without condition normalization. In engineering design, the voltage rating should first be determined on the basis of maximum bus voltage, regenerative-braking overvoltage and lifetime derating, then conduction and switching losses should be calculated against the full-operating-condition current distribution, and overshoot, ringing and dynamic current sharing should be verified using double-pulse testing. For traction inverters, short-circuit withstand capability, recommended gate voltages, body-diode operating limits and

junction-temperature-dependent parameters should also be checked. Such an evaluation converts the parameter sheet of a device into verifiable system design boundaries.

3. Electric Drive System Topologies and SiC Compatibility

3.1. Drive System Architecture and the Two-Level Inverter

A typical electric drive system consists of the battery pack, dc bus, motor controller, drive motor, reduction gear and cooling loop. There are two power switches per phase leg in the three-phase two-level voltage-source inverter (VSI), giving structural simplicity, a low device count and mature control; this remains the baseline topology for current traction inverters. For a 400 V platform, 650 to 750 V rated devices may be used; an 800 V platform typically requires 1200 V rated devices to satisfy switching overshoot and reliability derating requirements. In the two-level topology, SiC MOSFETs can directly reduce switching losses and are particularly suitable for operating regions with high bus voltage, light load and high speed [4,5].

A drawback of the two-level topology is that the output voltage step equals the full dc-bus voltage. The high dv/dt of SiC increases common-mode voltage, motor-terminal overshoot and bearing currents. If the gate resistance is increased to slow down switching, the efficiency advantage of SiC may be eroded. The design focus of a two-level SiC inverter is consequently not to pursue maximum switching speed but to determine an acceptable boundary among device losses, overshoot, EMI and insulation stress.

3.2. Multilevel and Open-Winding Topologies

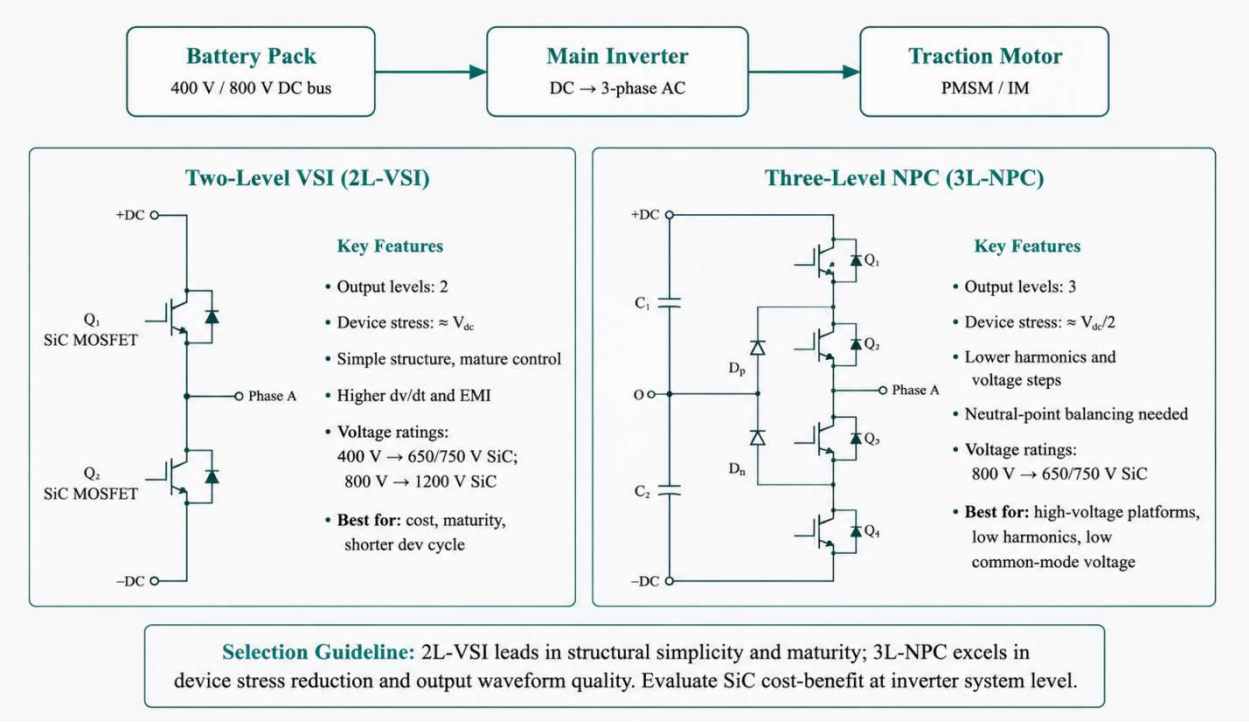

Figure 2. Typical electric drive system topologies and SiC device compatibility

Three-level neutral-point-clamped (NPC), T-type and active NPC topologies can reduce the voltage stress on devices to a fraction of the bus voltage while decreasing the output voltage step and current ripple. The trade-off is a higher switch count, more drive channels and greater complexity in neutral-point voltage balancing and fault control. For an 800 V system, a three-level topology can employ lower-voltage devices with superior switching performance; however, when 1200 V SiC MOSFETs can already satisfy a two-level design, whether the

multilevel approach is worthwhile should be jointly determined by efficiency, EMI, cost and control complexity.

An open-winding dual-inverter topology uses two inverters to drive the two ends of the motor winding, increasing dc-voltage utilization through voltage-vector combinations and giving a degree of fault tolerance. Dual-motor or multi-phase motor topologies can further enhance redundancy, but significantly increase the device count and control resources. By reducing the losses generated by the additional switching legs, SiC makes complex topologies more feasible; at the same time, multilevel and open-winding topologies can mitigate the EMI issues of SiC by reducing the single voltage step. The two concepts are thus complementary. Figure 2 compares these typical topologies and their SiC device compatibility.

3.3. Topology Selection and System Matching

Battery voltage, peak power, continuous power, motor insulation, cooling capacity and cost targets must all be considered in topology selection. The two-level full-SiC scheme has a low device count and mature control and is suitable for passenger vehicles pursuing high power density; the three-level scheme is more attractive for scenarios with high bus voltage, low harmonic distortion and stringent EMI requirements; hybrid topologies can allocate SiC to the high-frequency or high-loss legs to reduce device cost. Discrepancies often arise in the literature where one topology achieves higher rated-point efficiency while its full-operating-condition energy-consumption advantage is insignificant; the root cause is usually differences in switching frequency, modulation strategy and vehicle mission profile. Table 2 summarizes the key features and applicable scenarios of these topologies. SiC topology compatibility should therefore be evaluated on the basis of efficiency maps rather than a single rated operating point.

There is also no simple one-to-one correspondence between a high-voltage platform and SiC. Raising the bus voltage reduces current and wiring losses at the same power level and expands the voltage margin in the high-speed region, but the switching energy of the device, insulation clearance, partial discharge and common-mode interference may increase with voltage. If the motor windings and connectors are not upgraded in parallel, the inverter efficiency gain may come at the expense of insulation reliability. Hence, the advantages of using SiC in an 800 V system typically stem from the combined effects of current reduction, fast switching and the charging architecture, rather than solely from a higher rated voltage. Topology justification should simultaneously cover minimum and maximum battery voltage, peak regeneration conditions, fault states and cooling-system capacity, and should report device utilization and protection margins.

Table 2. Comparison of typical electric drive inverter topologies

Topology	Key Features	SiC Compatibility Advantage	Main Constraints	Applicable Scenarios
Two-level VSI	Few devices; mature control	Directly reduces switching loss and cooling burden	High dv/dt and common-mode interference	Mainstream 400/800 V passenger EVs
Three-level NPC / T-type	Small voltage step; lower harmonics	Can use lower-voltage, higher-speed devices	More devices; complex neutral-point balancing	High-voltage and EMI-sensitive platforms
Open-winding dual inverter	Rich voltage vectors; fault-tolerance potential	SiC mitigates additional leg losses	Dual supply / common-mode and control complexity	High-performance or redundant drives
Si/SiC hybrid	Si handles low-freq high power; SiC handles high-freq	Trade-off between cost and efficiency	Complex control and device stress allocation	Cost-constrained transitional solutions

4. SiC Inverter Control Strategies

4.1. Control Objectives and Loss Formation Mechanisms

Within the constraints of dc-bus voltage limits, torque demands and motor thermal boundaries, the electric drive control system must achieve fast, smooth and efficient energy conversion. Permanent-magnet synchronous motors (PMSMs) typically employ rotor field-oriented control, decomposing the stator current into flux and torque elements and combining maximum-torque-per-ampere (MTPA), field-weakening and voltage-utilization optimization to cover the range from low-speed high-torque to high-speed constant-power operation. SiC reduces inverter switching losses but does not automatically reduce motor copper loss, iron loss or mechanical loss; the control strategy must therefore shift from maximizing inverter efficiency to minimizing total drivetrain loss.

The switching loss of a traction inverter is related to the switching energy of the device, the switching frequency, bus voltage, phase current and junction temperature, while conduction loss is influenced by current, duty cycle and $R_{DS(on)}$. In the low-speed high-torque region, the current is large and the share of conduction loss rises; in the high-speed light-load region, switching loss and iron loss become more significant. A fixed switching frequency therefore cannot maintain optimality across all operating conditions.

4.2. Modulation Strategies and Switching-State Optimization

Space-vector pulse-width modulation (SVPWM) fully utilizes the dc-bus voltage, offers good harmonic performance and straightforward digital implementation, and is the common method in traction control. Continuous PWM distributes switching events evenly and gives smaller torque ripple, but every carrier cycle may involve commutation of each phase leg; discontinuous PWM (DPWM) clamps one leg during specific sectors, reducing the number of switching events and is suited to reducing inverter losses at high current. The trade-off is a change in common-mode voltage and the distribution of harmonics, which must be jointly evaluated against motor noise and EMI requirements.

At high modulation indices and in the field-weakening region, overmodulation can extend the voltage output range, but current harmonics and control nonlinearity increase. Multilevel inverters further require selection among redundant vectors to balance the neutral-point voltage and device losses. The lower switching losses of SiC devices give greater headroom for model-predictive control and high-frequency modulation, but controller sampling, computational delay and current-sensor bandwidth may still be limiting factors.

4.3. Switching-Frequency Efficiency Trade-off

Raising the switching frequency reduces current ripple, lowers torque pulsation and shrinks filter size, yet total losses do not decrease monotonically. Conduction loss is insensitive to switching frequency, while switching loss increases approximately linearly with frequency; at the same time, smaller ripple may reduce some motor additional losses. Total loss typically exhibits a minimum region determined jointly by operating condition, device and motor, rather than monotonically improving with higher frequency, as the normalized trend in Figure 3 illustrates. SiC shifts the minimum-loss point toward higher frequencies, but the high-frequency end remains constrained by output capacitance, drive losses, magnetic elements and EMI [5].

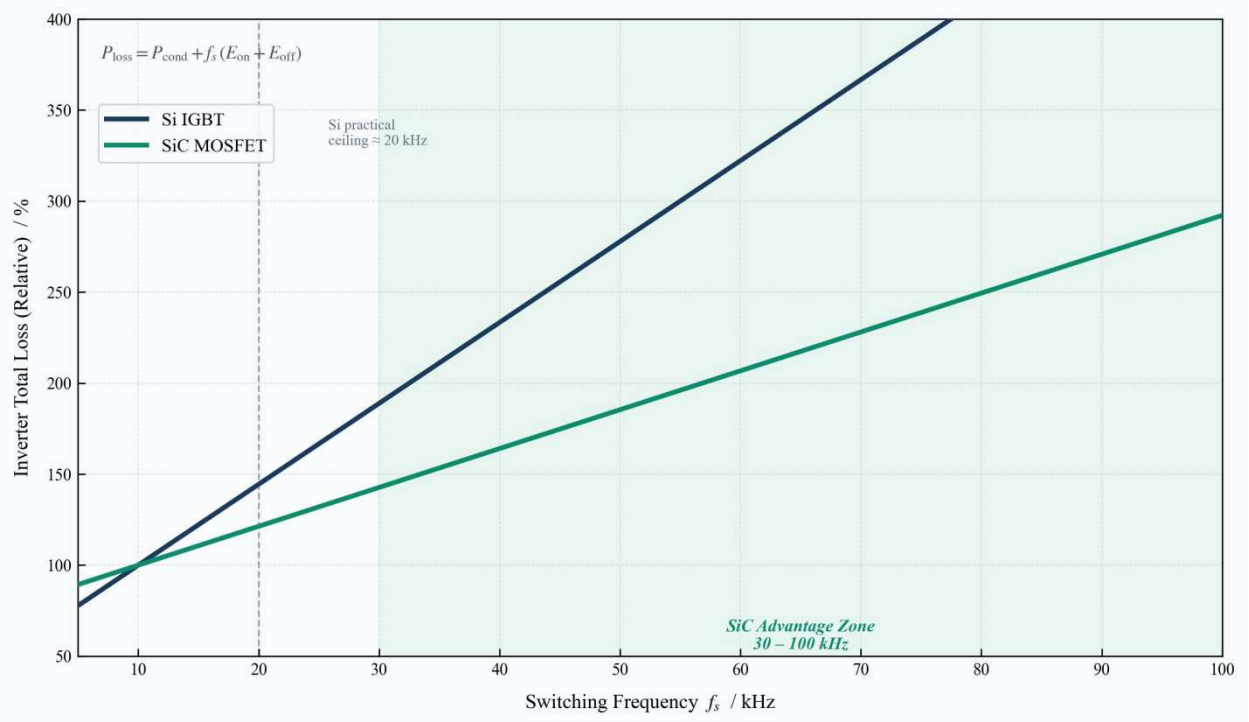

Figure 3. Normalized loss trends as a function of switching frequency

4.4. Device-Control Co-Design Strategies

For full-operating-condition optimization, the switching frequency and PWM mode can be selected online on the basis of speed, torque, bus voltage and junction temperature: at low speed and high current, a lower frequency or DPWM is used to reduce switching events; at high speed and light load, the frequency is increased subject to EMI and motor-loss constraints. Dead-time compensation and synchronous rectification can reduce third-quadrant body-diode conduction and improve voltage error near zero current. For paralleled SiC MOSFETs, symmetrical drive, Kelvin source connections and dynamic gate-resistance control are also needed to suppress transient current imbalance.

Active gate driving can vary the gate current during different phases of turn-on and turn-off, controlling di/dt, dv/dt and voltage overshoot independently. Compared with a fixed gate resistor, it has the potential to reduce the excessive speed derating set to accommodate worst-case conditions, but adds drive-circuit, sensing and calibration complexity. The proper control objective should be minimum total loss subject to safe-operating-area, EMI-limit and motor-insulation requirements, not the fastest switching speed achievable under datasheet conditions.

Validation on real-time control platforms and physical systems is ultimately required for the effectiveness of control strategies. Offline loss models should be corrected with double-pulse data at various temperatures, voltages and currents; motor models must account for magnetic saturation, parameter thermal drift and high-frequency additional losses. Efficiency maps over the torque-speed plane can then be obtained on a dynamometer, and energy consumption can be calculated using representative vehicle mission profiles rather than reporting only a single rated operating point. For online variable-frequency and active-drive approaches, mode-switching torque disturbance, sampling delay, fault degradation and EMC margins should also be verified. Only when control benefits are consistent across model, bench and mission-profile levels can the added algorithmic and hardware complexity be justified.

5. System Integration, Thermal Management, and Reliability

5.1. SiC Power Module Packaging and Integration

In conventional power modules, a vertical thermal path of chip, solder layer, DBC or AMB ceramic substrate and baseplate is typically employed, with aluminum wire bonds providing top-side chip interconnection. This structure is process-mature, but wire bonds and solder layers are susceptible to fatigue under thermal cycling, and the parasitic inductance of the power loop amplifies the overshoot produced by SiC high-speed switching. Automotive SiC modules have therefore progressively adopted silver-sintered die attach, copper wire or copper-clip interconnects, Si_3N_4 AMB substrates, planar interconnects and double-sided cooling [6].

The electrical and thermal objectives of packaging optimization are not fully aligned. Shortening the power loop lowers the parasitic inductance, but a compact layout raises thermal coupling; eliminating wire bonds helps reduce inductance and improve the cycling lifetime, yet places higher demands on coefficient-of-thermal-expansion matching and manufacturing consistency. Discrete-device paralleling can lower module procurement cost and increase structural flexibility, but requires resolving static and dynamic current sharing, PCB current carrying and heat-dissipation path issues. Packaging solutions should therefore be selected according to power level, cooling method and volume-manufacturing capability, rather than ranked solely by minimum parasitic parameters.

5.2. Thermal Path Design and Cooling Technologies

Steady-state junction temperature can be approximately calculated from the coolant temperature, device losses and cascaded thermal resistances: $T_j \approx T_{coolant} + P_{loss} \times \Sigma R_\theta$, where T_j is the junction temperature, $T_{coolant}$ is the coolant temperature, P_{loss} is the device power loss, and R_θ is the thermal resistance. Actual vehicle duty cycles are highly transient and additionally require Foster or Cauer thermal networks to describe the thermal capacitances of the chip, sinter layer, ceramic and cold plate. SiC reduces losses and permits higher junction temperatures, but high-power-density designs often shrink chip and module area, raising the local density of heat flux; if the cold plate is designed on the basis of average loss only, transient temperature excursions during acceleration, hill climbing and near-stall conditions may be underestimated [9].

Pin-fin cold plates, microchannels and jet impingement can enhance convective heat transfer, while double-sided cooling shortens the thermal path and increases the effective heat-dissipation area, thereby reducing junction temperature and chip-to-chip temperature variation [9]. Enhanced cooling may, however, increase pumping power, pressure drop, sealing risk and manufacturing cost; low thermal resistance does not equate to uniform temperature distribution. Thermal design should simultaneously evaluate peak junction temperature, inter-chip temperature difference, cooling-system power consumption and the temperature-cycling amplitude under the mission profile.

From the perspective of packaging and cooling schemes: wire bonding with single-sided cooling is process-mature, cost-effective and supply-chain-friendly, suitable for medium-power and cost-sensitive platforms, but has higher parasitic inductance and wire-bond and solder fatigue risks; planar copper interconnects offer low inductance, high current-carrying capacity and facilitate chip paralleling, suited for high-frequency, high-power-density modules, but require higher process consistency and thermal-stress control; silver-sintered die attach is high-temperature capable with high thermal conductivity and significant power-cycling lifetime potential, suitable for high-junction-temperature and long-life modules, though sintering pressure, porosity and material cost must be controlled [6].

Double-sided direct cooling shortens the thermal path and reduces junction temperature and temperature difference, applicable to high-heat-flux integrated electric drives, but increases insulation, sealing and structural complexity; microchannel or jet-impingement cooling gives strong heat-transfer capability and hotspot-suppression potential, suitable for high-peak-power or research applications, at the cost of increased pressure drop, pumping power, clogging risk and fabrication cost. No scheme is thus absolutely superior independently of application boundaries; trade-offs are required among thermal performance, reliability, manufacturing cost and system energy consumption [9].

5.3. Principal Failure Mechanisms and Reliability Assessment

SiC module reliability encompasses both intrinsic chip degradation and package fatigue. At the chip level, the main concerns are gate-oxide threshold-voltage drift, body-diode bipolar degradation, avalanche damage and short-circuit damage; at the package level they include wire-bond heel cracking, sinter or solder fatigue, ceramic-substrate cracking and interface delamination [7,8]. Because different failure mechanisms are jointly influenced by temperature, gate voltage, current and mechanical vibration, a single high-temperature reverse-bias or power-cycling test cannot fully represent the vehicle lifetime.

Chip, drive and system coordination is particularly demanded by short-circuit protection. SiC MOSFETs exhibit high short-circuit current density and short withstand times; protection circuits must rapidly identify anomalies while using soft turn-off to limit the overvoltage caused by stray inductance [7]. Overly fast protection may increase false triggering, while too-slow protection may damage the gate oxide, source metallization or the junction region. Negative gate-voltage turn-off and Miller clamping can reduce spurious turn-on, but an excessively low turn-off voltage may also increase gate-oxide stress; parameters must be determined by combining device data with lifetime testing.

Reliability assessment should transition from fixed-stress testing to mission-profile-driven approaches. First, device losses and junction-temperature sequences are derived from vehicle speed, torque, coolant temperature and ambient temperature; cycle-counting and lifetime models are then used to estimate package damage, combined with gate-bias, short-circuit and humidity-heat stress for multi-mechanism cross-checking. Online junction-temperature estimation and threshold or on-resistance monitoring can give health-management information, but the measured quantities are susceptible to switching noise and operating-point variations, requiring calibration and uncertainty analysis [8].

A contradiction in current reliability research is that accelerated testing facilitates obtaining failure data within limited time, yet may alter the actual failure mechanism. For example, excessively high junction temperatures, large temperature swings or extreme gate voltages can shorten test duration, but the resulting lifetime model may not apply to the lower stress, longer duration and multi-factor superposition encountered in vehicles. Different packaging materials and chip structures should not share the same set of lifetime parameters. To improve comparability, test reports should fully specify sample size, failure criteria, stress waveform, cooling boundary conditions and statistical distributions, and should distinguish parameter drift, functional failure and catastrophic failure. Automotive qualification gives basic entry conditions; OEMs still need to perform element-level and system-level verification on the basis of actual mission profiles.

5.4. System-Level Co-Design

The high power density of SiC electric drive systems arises from the mutual reinforcement of device, packaging, control and cooling, accompanied by the mutual propagation of constraints. Increasing switching speed reduces switching energy but increases overshoot and EMI; reducing chip area lowers material cost but raises current density and the density of heat flux;

enhanced cooling can reduce average junction temperature, but if the control strategy induces larger temperature swings, power-cycling lifetime may not improve in step. The co-design depicted in Figure 4 should take mission profiles as input and evaluate electrical losses, parasitic parameters, thermal fields, mechanical stress and health status within a unified iterative framework.

We argue that the most important change during the system-integration stage is shifting the evaluation metric from peak efficiency to full-operating-condition energy consumption and lifetime benefit. The design process should first establish bus voltage, power and safety boundaries; then jointly optimize chip count, package parasitics, gate drive, PWM strategy and cold-plate structure; and finally close the loop through double-pulse, dynamometer, EMC, thermal-cycling and power-cycling testing. Only under the same mission profiles and boundary conditions can one judge whether the efficiency, volume and reliability benefits of SiC justify the device and packaging cost.

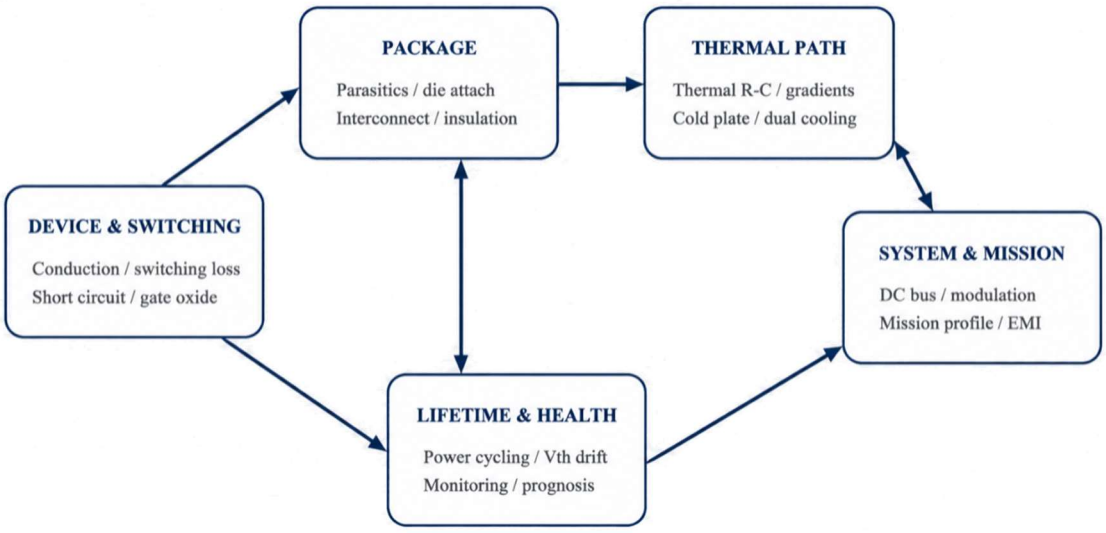

Figure 4. Electrical-thermal-reliability co-design relationships in SiC electric drive systems

6. Challenges and Future Outlook

6.1. Cost and Supply-Chain Bottlenecks

Long SiC substrate growth cycles, limited epitaxial efficiency and challenging defect control are the main reasons why device cost exceeds that of Si counterparts. Scaling has driven prices down, yet automotive-grade devices still require rigorous screening and reliability qualification; actual costs are jointly influenced by wafer yield, chip area and module packaging [4]. The industry transition from 150 mm to 200 mm wafers theoretically increases the area of the wafer by approximately 78%, but per-qualified-chip cost will decrease only if warp, epitaxial uniformity and the density of defects improve simultaneously. The key contradiction is the coexistence of the device price premium and system energy-saving benefits. We argue that cost is a structural barrier to full SiC adoption, but the breakeven point should be assessed using lifecycle cost composed of inverter, cooling and whole-vehicle energy consumption, rather than requiring device prices to match those of Si IGBTs.

6.2. Gate Oxide, EMI, and Short-Circuit Protection

Gate-oxide reliability has evolved from the question of whether the device can function to whether threshold-voltage drift over the vehicle lifetime can be predicted. Degradation results

differ across manufacturers, device structures and stress methods, indicating the need to map high-temperature gate-bias tests to real mission profiles [7,8]. Regarding high-speed switching, the large dv/dt and di/dt of SiC exacerbate overshoot, common-mode current and conducted and radiated emissions; increasing gate resistance suppresses noise but adds loss. We judge that EMI is primarily an engineering problem solvable through low-parasitic layout, filtering and active drive, but the objective should be meeting vehicle-level electromagnetic compatibility while retaining verifiable efficiency benefits.

The narrow short-circuit protection window is an important system-level threshold for traction applications. Fast desaturation detection, soft turn-off and current-limiting drive have well-defined technical paths, but faster detection increases false-trigger risk and circuit complexity [7]. Future efforts should therefore not merely pursue the longest short-circuit time of a single device but should adopt as the verifiable criterion that the minimum device withstand time exceeds the sum of detection, logic and turn-off delays with sufficient temperature and aging margins.

In summary, cost and supply chain represent structural challenges; the core tension lies between device price premiums and system-level benefits. Primary improvement paths include 200 mm wafers, higher yields, volume production and standardized packaging; assessment should consider both per-qualified-chip cost and total system lifecycle cost. Gate-oxide reliability straddles fundamental research and engineering application; the contradiction is that low on-resistance and long-term stability are difficult to improve simultaneously, requiring interface processing, gate-voltage derating and online monitoring, with threshold-voltage drift and lifetime distribution after mission-profile exposure serving as evaluation metrics [8].

High-frequency EMI is an engineering challenge in which the contradiction manifests as the trade-off between low switching loss and interference or insulation stress; low-parasitic design, filtering and active drive can bring improvement, and the ultimate goal should be that EMC margin, voltage overshoot and efficiency all meet their targets simultaneously. Short-circuit withstand capability is a system-level challenge, with the core contradiction between high power density and a limited protection window, requiring the combination of current-limiting cells, fast detection and soft turn-off such that the minimum device withstand time exceeds the total protection delay with the necessary margin [7]. These metrics link device performance, protection design and system verification, and can serve as a unified verification boundary for different SiC electric drive solutions.

6.3. Material, Device, and Packaging Trends

Looking ahead, the first priority is the co-maturation of 200 mm wafers, epitaxial defect control and wafer-thinning processes; the second is novel trench-gate, integrated-SBD and cell structures that balance low on-resistance with short-circuit robustness; the third is the coordinated development of silver sintering, copper interconnects, low-inductance planar packaging, double-sided cooling and direct cooling [6,9]. The key contradiction across these directions is that performance improvement may increase gate-oxide field stress, the density of heat flux or manufacturing difficulty. We argue that wafer size should be verified by per-qualified-chip cost, device structures should simultaneously report conduction, switching, gate-oxide and fault-robustness metrics, and advanced packaging should be evaluated by power-cycling lifetime and batch consistency rather than solely comparing minimum thermal resistance or parasitic inductance of laboratory prototypes.

6.4. System Architecture and Application Outlook

At the vehicle-architecture level, SiC and GaN may form a division of labor by power and frequency: SiC for high-voltage high-power traction, GaN for higher-frequency onboard charging and dc-dc stages. Data-driven methods will also be applied to thermal-state estimation,

fault diagnosis, lifetime prediction and adaptive gate control, but algorithms must be constrained by device physics, safety boundaries and real-vehicle data. As 800 V and higher platforms develop, the application space for 1200 V and 1700 V SiC devices in high-power passenger and commercial vehicles will expand, while insulation, partial discharge, EMI and protection challenges will also intensify.

SiC will not fully replace Si IGBTs in the short term. Vehicle platforms with high voltage, high power density and limited cooling space are more likely to capture system-level benefits; cost-sensitive and lower-power platforms may still employ Si IGBTs, hybrid modules or partial SiC solutions. What future research most needs are unified comparison benchmarks, efficiency and lifetime data under public mission profiles and an electrical-thermal-EMI-reliability-cost joint optimization methodology. The long-term competitiveness of SiC will depend on whether material advantages can be stably converted into whole-vehicle lifecycle value.

Verifiable research directions specifically include: establishing device and module loss databases under unified bus, current, junction-temperature and switching conditions; developing mission-profile lifetime models covering urban, highway, hill-climbing and high- and low-temperature environments; studying the coupling among protection actions, gate degradation and package aging; incorporating cooling pumping power, filter volume and device cost into system optimization; and establishing confidence intervals for online health indicators and remaining useful life prediction. All of these directions should specify reference prototypes, error ranges and failure criteria, and should avoid equating simulation results or short-duration efficiency improvements with long-term whole-vehicle benefits. Only by forming reproducible test benchmarks and cross-level data closed loops can the industry delineate more accurately the applicability boundaries of full-SiC, hybrid-SiC and conventional Si solutions.

7. Conclusion

A systematic review of the application of SiC power devices in EV electric drive systems has been presented, organized around 4H-SiC materials and devices, drivetrain topologies, inverter control, packaging and thermal management, and reliability. The analysis shows that the core value of SiC is not merely a reduction in individual switch losses but, through its high-voltage, high-frequency and high-temperature capabilities, the enablement of holistic optimization of the inverter, cooling system and drivetrain assembly. System-level benefits depend on the coordinated design of bus voltage, vehicle mission profile, topology, modulation, drive, parasitic parameters and thermal path, and cannot be obtained automatically by device substitution.

SiC currently possesses the technological foundation for large-scale application in high-performance traction drives, but the development focus is shifting from performance demonstration to cost control and long-term reliability. EMI caused by high-speed switching, the narrow short-circuit protection window and package fatigue under high heat flux demand coordinated design of device, drive and cooling. In the future, larger wafers, novel device structures, advanced packaging, health-aware control and heterogeneous device architectures will continue to expand the applicability of SiC, while Si IGBTs will remain competitive on cost-sensitive platforms. The next phase of competition in SiC electric drive systems will hinge on whether material and device advantages can be translated into verifiable whole-vehicle efficiency, reliability and lifecycle economics.

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