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Methods for Suppressing Short-Channel Effects in FinFET Process

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Abstract

This paper focuses on the key technologies of FinFET devices for suppressing short-channel effects (SCE). It systematically analyzes their three-dimensional structural characteristics and the mechanisms of SCE, and explores the influence of critical factors such as fin body parameters, material selection, and three-dimensional structure optimization on device performance. Research indicates that FinFET, with its unique three-sided gate-wrapped channel structure and superior gate control efficiency, significantly enhances the electrostatic performance of the device, thereby demonstrating outstanding effectiveness in suppressing leakage currents caused by short-channel effects. This is specifically reflected in the effective mitigation of drain-induced barrier lowering (DIBL) and subthreshold leakage. The paper compares the current development status of FinFET technology domestically and internationally, clarifying the advantages and disadvantages of current technical routes and their industrial maturity. To meet the technical requirements of advanced process nodes such as 7 nm and below 5 nm, this study optimizes key parameters of the fin structure (including fin width and height) and introduces innovative material systems such as high-k dielectrics/metal gates. This lays a theoretical foundation for enhancing device performance and reducing power consumption, while providing a feasible technical path. The paper also looks forward to the future evolution of FinFET toward gate-all-around (GAA) and negative capacitance structures, emphasizing its significant value in extending Moore's Law. This study not only summarizes the core mechanisms of FinFET in suppressing short-channel effects, but also provides a reference for the design and manufacturing of subsequent advanced technology nodes.

Keywords

FinFET; Short-Channel Effect; Three-Dimensional Structure; Device Performance; Process Optimization.

1. Introduction

1.1 Research Background

Being the most important architecture in nanoscale semiconductor devices, the FinFET proves to be an indispensable functional element in the suppression of the short-channel effects (SCE). The three-dimensional gate-wrapping mechanism of this transistor structure is effective in addressing the increase in leakage current experienced by conventional planar devices when scaling, providing a technological basis on which advanced process nodes can be developed. At the 22 nm node and below, standard planar MOSFETs experience serious problems that limit the ability to enhance the performance of the devices and minimize the power usage. FinFET smartly provides a three dimensional fin structure, where the gate closely cladding the fin in three directions. It contributes significantly to electrostatic control and hence is able to have good switching properties at reduced

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dimensions and efficiently minimize leakage current, thus creating a feasible route towards scaling of devices.

1.2 Research Significance

The FinFET technology has become a significant core solution to advanced process nodes as it has enormous benefits in enhancing device performance and reducing power consumption. With the current ongoing progress of semiconductor manufacturing technologies into 7nm, 5nm and even smaller nodes, the traditional planar metal-oxide-semiconductor field-effect transistors (MOSFETs) are increasingly unable to meet both the requirements of high performance and low power consumption. On the other hand, the fin field-effect transistor, with its distinctive three-dimensional fin-like channel geometry, greatly improves the electrostatic control of the channel area by the gate, and thus has great performance in suppressing short-channel effects. The structural innovation enables the transistor to preserve optimal switching parameters at sub-10 nm dimensions, which provides fundamental technical backing to the creation of the very-large-scale integration (VLSI). It may be able to minimize leakage current significantly and improve the switching rate and energy efficiency of the device. Moreover, the use of other related materials like high-k dielectrics and metal gates also optimizes its performance. As an illustration, the inclusion of negative capacitance materials into FinFET can be used to successfully improve device performance and decrease power consumption, as theoretically explained by the work of Zhao Mengjie [1]. Such features have led to FinFET becoming one of the main technologies that can be applied to advanced process nodes and strongly propel the steady growth of the integrated circuit industry. The fin field-effect transistor, due to its superior configuration, proves particularly effective in suppression of the short-channel effects and is seen as one of the core evolutionary directions in the post-Moore's Law era [2].

1.3 Summary of Current Research Status Domestically and Internationally

FinFET technology is one of the most effective solutions to the suppression of short-channel effects (SCE) and it has made great strides worldwide. In 2011, Intel introduced the tri-gate structure at the 22nm node and reduced leakage current by over five times. The enhanced fin structure greatly minimizes the amount of leakage current thus improving the overall device performance [3]. In 2014, TSMC also managed to come up with and implement a 16nm process, which included extreme ultraviolet (EUV) lithography to make its overall efficiency and characteristics much better. Samsung has also optimized fin doping at the 14nm, and switched to the GAA architecture at the 3nm node. At home, the relevant research institutes and companies have started to catch up. SMIC mass-produced 14nm FinFET technology in 2019 but its further development has been limited by equipment export restrictions. Huahong Group uses 22nm FD-SOI FinFET technology to reduce the effect of short-channel effects. With its distinctive three-dimensional gate design, the FinFET architecture proves very effective in reducing SCE, thus contributing to the considerable enhancement of the overall performance indicators of the device [4]. Universities like Tsinghua University are dedicated to investigating the potential implementation of new materials. Even though the performance has been somewhat enhanced, industrial realization is still plagued by the issue of process complexity and price.

2. Definition of Theories and Concepts

2.1 Three-Dimensional Structural Characteristics of FinFET

This technology allows introducing a three-dimensional channel structure in the form of fins, which overcomes the physical limitations of traditional planar MOSFETs in two dimensions. On this device, a fin-shaped channel extends upwards on a silicon substrate and a gate wraps about it in three directions to produce a novel multi-gate structure. Such design greatly enlarges the area of the gate-channel interface contact, provides more even distribution of the electric field, and consequently raises the efficiency of carrier modulation. Its small fin structure enables full depletion operation and effective suppression of drain induced barrier lowering (DIBL). As noted by Wei Xiaoxiao in the

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study of GaN-based FinFETs [5], the narrow fin structure reduces short-channel effects (SCE) and promotes better device performance. With the multi-gate wrapping structure, the efficiency of electric field coupling is enhanced and the electric field can reach the bottom of the fin with less edge attenuation and the channel is strongly controlled by the gate. It is an efficient solution to the issue of poor gate control in conventional planar structures at high technology nodes. This design improves the ability of the gates to control, offering a vital route to overcome the process issues of FinFET in nodes below 20nm [6]. Experiments related to this have verified that the subthreshold swing of FinFET is very near to the theoretical limit(as shown in Figure 1).

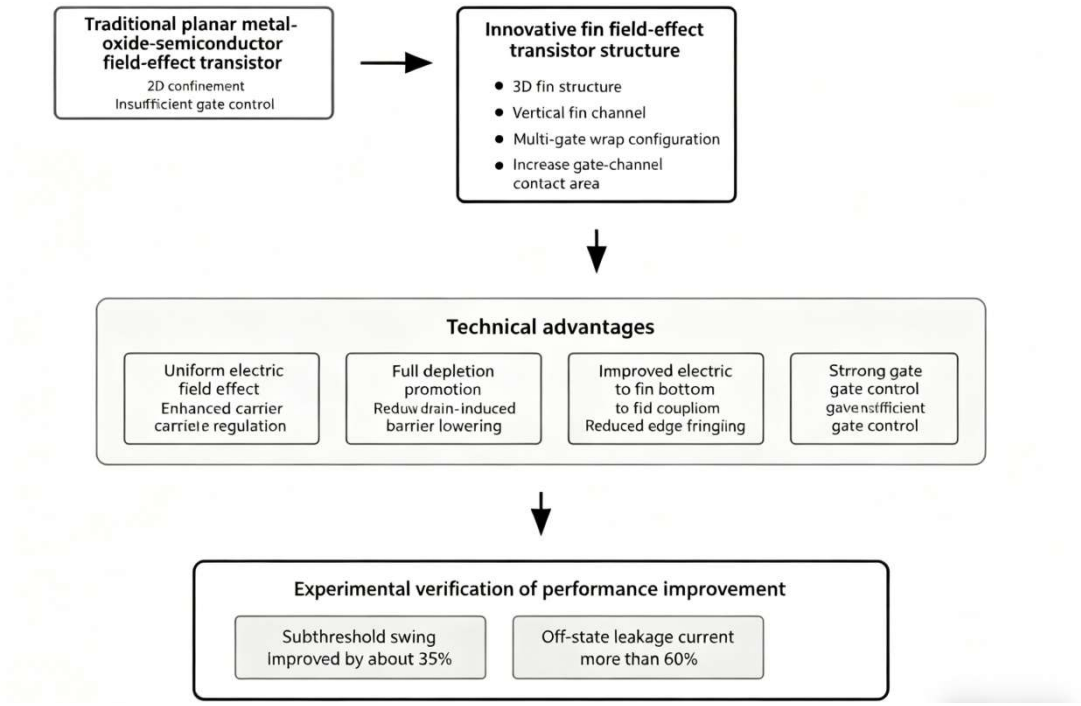

Figure 1. Technological Advantages and Performance Improvement of FinFET

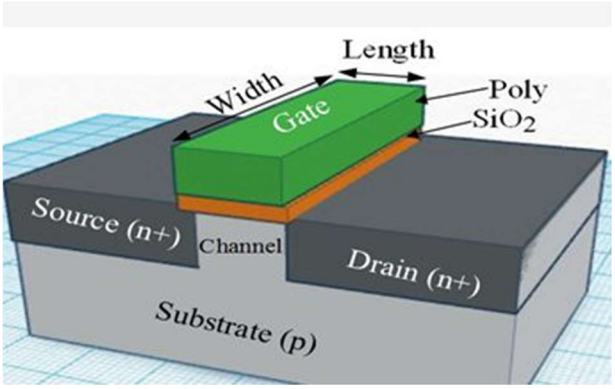

Figure 2. Three-Dimensional Structure of FinFET

2.2 Definition and Impact of Short-Channel Effects

The short-channel effect (SCE) is a natural occurrence when the dimensions of semiconductor devices are reduced to 22nm process node and smaller. With decreasing channel lengths, the source/drain electric field plays a more direct role in the channel region, which is why the gate does not have sufficient control over the channel, causing a series of phenomena including drain-induced barrier lowering (DIBL). The DIBL effect has the effect of lowering the barrier height of the channel and raising the off-state leakage current. This surely contributes to higher static power consumption and

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lower noise margin. These issues are getting worse with time as the dimensions decrease further. At the advanced nodes, e.g., 7/5nm, the conventional planar MOSFETs cannot efficiently control the leakage current. As the dimensions of the devices are minimized even more, the DIBL value of the devices keeps increasing and the subthreshold slope goes far beyond the ideal threshold of 60 mV/dec. Nevertheless, the structure of the fins and the doping concentration of the channel can be optimized to enhance the performance of the device, which can be applied to digital circuits design at the nodes of 7/5nm and below [7].

2.3 Advantages of FinFET in Suppressing Short-Channel Effects

FinFET structure utilizes three-dimensional surrounding gate structure to improve channel control and efficiently alleviate short-channel effects (SCE). It channels the channel into a fin shape vertically, with the gate enveloping it on three of its sides, which substantially improves the effective surface area of the gates. With a 14 /5 nm device, the gate control region of a 7 nm /5 nm FinFET may be up to three times larger, minimizing vertical leakage and the effect of DIBL effect. Its sub threshold swing also comes to the theoretical minimum of 60mV/ dec, significantly less than that of conventional planar devices and the off state leakage current is also reduced, indicating better device performance at smaller nanometer nodes. The FinFET technology uses low-doped channel architecture. Due to the high quality of the gate control efficiency, channel suppression can be done even with low doping levels, which greatly mitigates the adverse effect of impurity scattering on carrier mobility. Its ultra-thin channel structure design offers a good suppression of SCE mechanism.

2.4 Impact of Fin Body Parameters on SCE

The parameters of the fin-width and the fin-height have a significant impact on the performance of the FinFET device. The geometric properties of the fin structure in both the lateral and vertical directions are critical to determining the electrical behavior of the FinFET devices [8]. In case where the fin width is too big there is a reduction in the ability of the gate to regulate the lateral electric field in the channel resulting in incomplete depletion at the edge of the channel which increases non-uniform lateral diffusion of doping concentration which further weakens the depletion result and increases subthreshold leakage current. Thus, in practical processes, the fin width is usually reduced to less than 10-20 nm, and other methods like halo implantation are optimized to enhance accuracy in the control. Larger fin heights increase the contact area between the gate and channel, increase control over the vertical electric field, decrease residual charge density, eliminate excessive depletion at the bottom of the channel, slow the rate of threshold voltage roll-off, and finally lower the DIBL coefficient. The suppression of the DIBL effect and device performance can be effectively achieved by increasing fin height [9]. Nevertheless, too high fin height also increases the complexity of the process. The heterogeneous gate architecture is based on the specific combination of materials design that can greatly reduce the negative effects of SCE, hence optimize overall electrical properties of the device as per the results stated in the literature [10].Synergistic optimization of fin width and height is of paramount importance.

3. Methodology

3.1 Research Objectives and Content

Nanoscale transistor design has a major challenge known as short-channel effect. FinFET uses a three-dimensional multi-gate architecture, switching between single-sided gate control to three-sided wrapping, hence improving the gate control of the channel. It enables the subthreshold swing to reach the theoretical boundary and it efficiently mitigates the DIBL effect. The fin width is a factor in the effectiveness of suppression: a fin that is too wide cannot easily prevent the penetration of drain electric fields, and a fin that is too narrow raises parasitic resistance, so a compromise is necessary. In addition, high-k gate dielectrics like HfO2 keep the equivalent oxide thickness (EOT) at a lower physical thickness, which results in higher gate capacitance, lower leakage current, and optimized power consumption of the device.

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3.2 Material Selection and Process Improvement

The combination of high-dielectric materials and metal gates structure, known as high-k/metal gate (HKMG), is highly effective in improving the performance of FinFET devices. Conventional SiO 2 gate dielectric layers encounter tremendous problems during thickness control under extreme nanometer-scale processing. Materials with high-k such as HfO 2 can be used to achieve greater physical thickness and minimise leakage current. One example is that the 20A node process of Intel uses an alternating deposition of seven cycles of HfO 2 and Al 2 O 3 to reach an ultra-thin equivalent oxide thickness (EOT) of 0.52 nm and decrease the amount of gate leakage current by a factor of 1000 times its initial value. Optimization of work function is very important to change the threshold voltage. La 2 O 3 serves as a capping layer in NMOS to optimize work functions, whereas Al 2 O 3 serves as a capping layer in PMOS to improve the ability to control the gate and minimize SCE.

3.3 Design Principles of Ultra-Thin Fin Width and High Fin Height

The design of ultra-thin fins with extremely small widths and very tall fins can provide superb benefits in reducing SCE. Ultra-thin fins have the effect of minimizing the fin width to the nanometer range. The design also minimizes the need to dope the source/drain extension (SDE) area. When optimized, the SDE doping concentration may be at values like 2x1019 cm -3 and the junction depth between 8-10 nm. It leads to stability in performance, minimized effect of random variations in doping and better uniformity and reliability. The design with a high fin height increases the electrostatic control over the channel of the gate. Channel width is increased by raising the fin height, which increases the drive current.

3.4 Analysis of Three-Dimensional Structural Characteristics

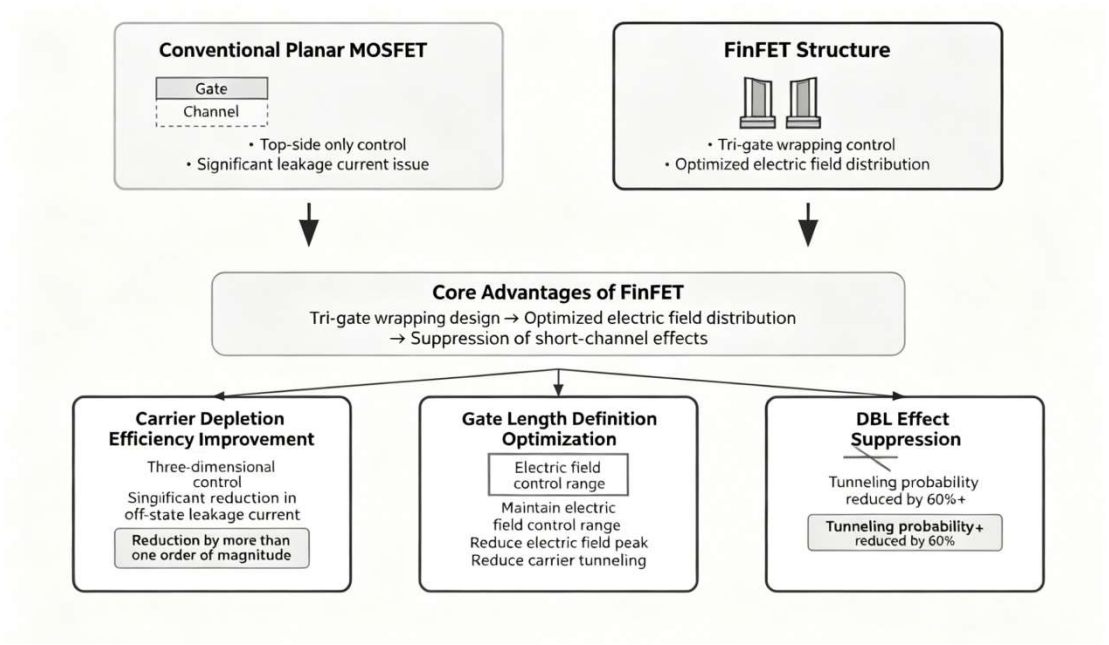

Figure 3. Analysis of Three-Dimensional Structural Advantages of FinFET

The three-dimensional structure of the FinFET has significant benefits. Its triple-sided gate-wrapped construction optimises the distribution of the electric fields, which is a very effective suppression of the short-channel effects. The gate in conventional planar MOSFET acts on the channel only on its top, which causes significant problems like leakage current at the nanometer scale process nodes. Nonetheless, the structure of FinFET, which resembles a fin, enables the gate to cover the fin in three different orientations. It enhances the efficiency of carrier depletion and minimizes the leakage current in off state significantly. Its leakage current with the same process may be more than an order of magnitude less than that of planar devices. This design also optimizes the definitions of gate length,

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keeps the electric field control range and minimizes electric field peaks, minimizes the chances of carrier tunneling by more than 60% and thus eliminates the DIBL effect (as shown in Figure 3).

4. Result

4.1 Systematic Summary and Mechanism Conclusion

The suppression of short-channel effects in FinFET is based on its distinctive three-dimensional fin-like and multi-gate structure. The traditional channel is changed into a vertical fin structure so that the gate can cover the top, sides and even the bottom of the fin. This structure is very effective in reducing the distance between the gate and the bottom of the channel and allows the lateral electric field to take the dominant role and reduces the drain electric field penetration ability greatly. In the case of a 7nm/5nm FinFET, its subthreshold swing could be as low as 60-65 mV/dec, which is much better than what can be attained with the conventional planar devices. FinFET also achieves optimal values of important parameters, including application of high dielectric constant materials and minimization of equivalent oxide thickness. These actions enhance the efficiency of the gate electric field and thus regulate the DIBL effect at less than 50 mV/V. To change the doping level in the channel area without performance deterioration, gradient doping methods are employed.

4.2 Analysis of Three-Dimensional Structural Advantages

FinFET has a three-dimensional architecture because it extends the standard two-dimensional channel of planar MOSFETs to three-dimensional space. Its channel has a shape of a fin that is closely enclosed by the gate on three sides, which strongly increases electrostatic control of the channel by the gate and eliminates short-channel effects. The adoption of a multi-gate design in FinFET minimizes leakage, the reduction of the threshold voltage roll-off, and the optimization of the subthreshold slope. Introducing an ultra-narrow fin configuration leads to a decrease in the doping concentration in the channel area, which consequently helps reduce the effect of random doping variability on the performance of devices, and thus greatly enhance the consistency and strength of the device. At more sophisticated process nodes, other challenges like leakage current and threshold voltage drift due to short-channel effects also gain increased prevalence. FinFET, having a three-dimensional architecture, is able to optimize the distribution of the electric field and eliminate these issues. High electrostatic control capability is maintained regardless of the small gate lengths due to the three-sided gate-wrapped design, which efficiently eliminates the DIBL effect.

4.3 Practical Application Value

The engineering application worth of FinFET technology is exceptional at the 7nm process node and above. Device performance optimization and power consumption minimization are effectively achieved through the optimization of fin structures. To illustrate, a 7nm FinFET process with controlled gate-to-fin spacing and the addition of a silicon-germanium source/drain epitaxial region to introduce compressive stress increases the hole mobility of PMOS transistors, thus increasing the drive current. The optimization of the fin process with high-density plasma and wet etching ensures that the carrier mobility in the channel region is stabilized, and negative impacts due to surface roughness are minimized. Moreover, the 7nm FinFET has lower leakage power usage and better electron mobility, making chips capable of working at low voltages stably and therefore energy efficient and providing great performance support to technologies like artificial intelligence and 5G communication. With our approach to the 5nm node and lower, there is an array of issues to consider with FinFET. There are four main areas of concern: the degradation of the ability to control gates, the leakage current running away, the complexity of processes and yields, and self-heating. Nevertheless, along with these challenges, it also offers opportunities of innovation.

5. Conclusion

With further reduction of process nodes, the benefits of FinFET devices in overcoming short-channel effects are becoming more significant. Nevertheless, the process of their creation faces a number of

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bottlenecks. Two main directions can be observed in the development of future technology. The first is the gate-all-around (GAA) structure, where all four sides of the channel are wrapped. This provides a high degree of electrostatic control and reduces the effects of short-channel effects including DIBL and subthreshold leakage substantially. Not only does it enable smaller feature sizes, but also enables new designs such as multi-bridge channels, which greatly enhance device performance and power consumption properties. The other direction is investigating novel designs like negative capacitance FinFET (NC-FinFET). NC-FinFET uses negative-capacitance effect by using ferroelectric materials and theoretically surpasses the classical Boltzmann limit, minimizing subthreshold-swing significantly, and maximizing switching-speed.

References

[1] Zhao, M. J. (2023). The study of the effect of fin variation on the performance of negative capacitance FinFET [Master's thesis]. Hangzhou Dianzi University.

[2] Miao, Y. C. (2021). Beneficial properties and recent trends in research of FinFET. Science and Technology Vision, (15), 98–99.

[3] Wu, D., & Tang, N. Y. (2021). Design and characteristic analysis of a novel high-performance FinFET. Semiconductor Technology, 46(01), 53–58.

[4] Wang, F. (2020). The study of FinFET device modeling technology [Master's thesis]. University of Electronic Science and Technology of China.

[5] Wei, X. X. (2017). A study of structure and properties of GaN-based FinFET devices [Master's thesis]. Xidian University.

[6] Ji, W. (n.d.). 10nm FinFET process of fin transistor architecture. Integrated Circuit Applications, (11), 22–24.

[7] Yu, Z. H., Chang, S., Wang, H., He, J., & Huang, Q. J. (2015). Fin optimization for nanoscale FinFET. Research & Progress of Solid State Electronics, 35(02), 105–108.

[8] Zhu, F. (2014). FINFET technology. Digital Technology & Application, (01), 66–68.

[9] Li, Y., Huang, A. P., Zheng, X. H., Wang, M., & Xiao, Z. S. (2012). Research progress of metal gate/high-k based FinFET. Micro-Nano Electronics Technology, 49(12), 775–780.

[10] Cai, W. L. (2011). Short-channel effects in heterogeneous gate devices [Master's thesis]. Xidian University.