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Analysis of Factors Affecting the Pixel Performance of CMOS Image Sensors

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Abstract

A CMOS image sensor is a semiconductor device that converts optical signals into electrical signals. It is widely used in various fields such as digital cameras, smartphones, security surveillance, medical imaging, and automotive electronics, serving as the core component of modern imaging technology. The surface of the sensor is composed of an array of millions of tiny photo sensitive units (pixels). Each pixel contains a photodiode and several transistors. This paper investigates the pixel performance of CMOS image sensors, analyzes the factors that affect pixel performance, and summarizes potential improvement methods.

Keywords

CIS; Temperature; Radiation; Pixel Structure; Manufacturing Process; Analysis and Summary.

1. Introduction

Vision is one of the primary ways humans perceive the world and acquire information. In the digital era, image sensors, serving as modern "electronic eyes," are the core devices for converting optical images into electrical signals. They are widely used in fields such as consumer electronics, security, healthcare, industry, autonomous driving, and aerospace, and their performance directly determines imaging quality and system capabilities. Therefore, a deep understanding of the principles, structures, and performance-affecting factors of image sensors is of crucial importance for the continuous innovation and application expansion of related technologies.

Image sensors are mainly divided into two major categories:Charge-Coupled Devices (CCD)andComplementary Metal-Oxide-Semiconductor Image Sensors (CMOS Image Sensors, CIS). The advantages of CCD technology lie in its high sensitivity, low noise, and high charge transfer efficiency (CTE), enabling a high dynamic range and high signal-to-noise ratio. Consequently, it has long been a leader in fields with extremely high image quality requirements, such as professional photography and scientific imaging.

However, CCD technology also has several limitations: complex manufacturing processes, high cost, large power consumption (especially at high speeds), limited readout speed, and low system integration (requiring numerous peripheral chips for support). These factors have restricted its widespread adoption in portable, low-power, highly integrated, and high-speed imaging applications.

It is against this backdrop that,since the 1990s, CMOS Image Sensors (CIS) have begun to flourish, demonstrating strong competitiveness and broad application prospects, thanks to the low cost, low power consumption, high integration, and higher readout speed potential brought by standard manufacturing processes[1].

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1.1 Research Background

With the growing sophistication and expansion of applications (such as ultra-high-definition video, computational photography, AR/VR, autonomous driving perception, Industry 4.0 visual inspection, etc.), the performance demands on CIS have become higher and more stringent. As the fundamental photosensitive unit of a CIS, pixel performance is the core foundation that determines the final imaging quality of the entire sensor. Amid trends toward pixel size miniaturization, functional integration, and performance maximization, it has become particularly important to deeply analyze and understand the various physical mechanisms and structural design factors that affect the performance of a single pixel.

This paper will focus on the core unit of the CIS-the pixel-and explore the main factors affecting its key performance indicators. This will be done from multiple dimensions, including physical mechanisms (such as photocarrier generation and collection, dark current sources, noise types), pixel structure design, and manufacturing processes, with the aim of providing a theoretical basis and reference for understanding CIS working principles, optimizing pixel design, and enhancing imaging performance.

1.2 Development Status of CIS Domestically and Internationally

CMOS sensorsnowoccupy over 90% of the market share, with imaging quality that fully rivals or surpasses that of CCDs, covering applications from consumer electronics to high-end scientific and medical fields. The international CIS industry started early, possesses deep technological expertise, and has a complete industrial chain, currently maintaining a leading position globally, with significant advantages in high-end technology R&D, core patent layout, and market share.

Sony: The definitive technology leader (40%-50% market share), with mastery of cutting-edge technologies such as stacked CIS (BSI + advanced processes), global shutter, 0.6μm ultra-small pixels, and SPAD/dToF (LiDAR). Dominates the markets for Apple/high-end smartphones, professional imaging, and automotive ADAS.

Samsung Electronics: The second-largest supplier (20%-30% market share). Leveraging its IDM production capacity, it has achieved breakthroughs with 0.56μm pixels and 200-megapixel high-resolution sensors. Its ISOCELL technology optimizes image quality for mid-to-high-end smartphones, while it also strengthens its presence in automotive and 3D sensing.

onsemi:The dominant player in automotive CIS, meetinghighdynamic range, LED flicker mitigation, and other automotive-grade requirements, and monopolizing the ADAS camera market.It also has a strong presence in the industrial machine vision and medical imaging sectors.

China's CIS industry is developing rapidly, dominating the global low-to-mid-range market and accelerating its push into the mid-to-high-end segment.

Will Semiconductor: Became the world's third-largest CIS design house after acquiring OmniVision. It boasts advanced technology, a comprehensive product line, and a high degree of internationalization, with products covering smartphones (all tiers), security, automotive electronics (aftermarket/some pre-installed), and laptops, making it a key player in domestic high-end replacement.

GalaxyCore: The global leader in mobile phone CIS shipments (by volume), dominating the low-to-mid-range market through extreme costcontrol and supply chainmanagement.The company is actively upgrading to the mid-to-high-end (mass-producing 0.7μm 32MP, 0.56μm 50MP sensors) and is building its own 12-inch BSI production line to enhance self-sufficiency.

SmartSens Technology: A global leader in security and surveillance CIS, with core strengths in excellent low-light performance (Starlight-level) and HDR. It innovated the SFCPixel™ technology and is now expanding into automotive electronics (in-cabin/ADAS surround view), machine vision, and smartphone markets.

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1.3 Main Content and Chapter Arrangement of This Paper

This paper focuses onthe factors for evaluating CIS pixel performance. It analyzes the manner and degree to which different factors affect the performance of CMOS image sensors and discusses possible optimization schemes.The chapter arrangement of this paper is as follows:

Chapter 1 is the introduction, primarily covering the project background and the development status of CIS domestically and internationally. Chapter 2 mainly introduces the characteristics of CIS, such as its structure and function. Chapter 3 primarily introduces the factors that this paper will focus on analyzing. Chapter 4 mainly analyzes the effects of different factors on CIS pixel performance and possible improvement schemes. Chapter 5 summarizes the research conducted for this project.

2. CIS Introduction

A CIS is a semiconductor device that converts optical images into electronic signals. Its core function is to use the photoelectric effect in silicon to transform incident photons into quantifiable electrical charge signals, thereby generating a digital image. A CIS is manufactured using standard complementary metal-oxide-semiconductor integrated circuit processes, integrating photosensitive units (the pixel array) and complex signal processing circuits onto a single chip, achieving a "System-on-Chip" (SoC).

A CIS structure can be broken down from top to bottom into the following key parts:

Optical Layer:

Microlens Array: Focuses incident light onto the photo sensitive area of the pixel, reducing light loss.

Color Filter Array (CFA): Uses a Bayer array or similar patterns, causing each pixel to be sensitive to only a specific band of light (R/G/B), enabling color imaging.

Metal Interconnect Layer: Located between the color filter and the photosensitive layer, it provides electrical connections for circuits within and between pixels (e.g., from pixels to row/column driver circuits).

Pixel Array Layer (Core Photosensitive Unit),where the basic unit is a single pixel, with the core being a photodiode, typically using a pinned photodiode structure. The mainstream architecture is the 4T pixel.

Silicon Substrate Layer

This is the supporting structure where photons are absorbed and converted into electron-hole pairs.

Back-Side Illumination (BSI) Optimization: Back-side thinning + anti-reflective coating allows light to directly enter the photodiode from the back, improving quantum efficiency.

Peripheral Circuitry Layer

Row Driver Circuitry: Controls pixel row selection, reset, and transfer timing.

Column Processing Circuitry:

Correlated Double Sampling (CDS): Eliminates reset noise and fixed-pattern noise.

Programmable Gain Amplifier (PGA) and Analog-to-Digital Converter (ADC): For signal amplification and digitization.

Timing Control Logic: Generates global clock and control signals.

Digital Signal Processing (DSP): Performs tasks like defect correction, noise reduction, auto exposure/white balance, and color interpolation.

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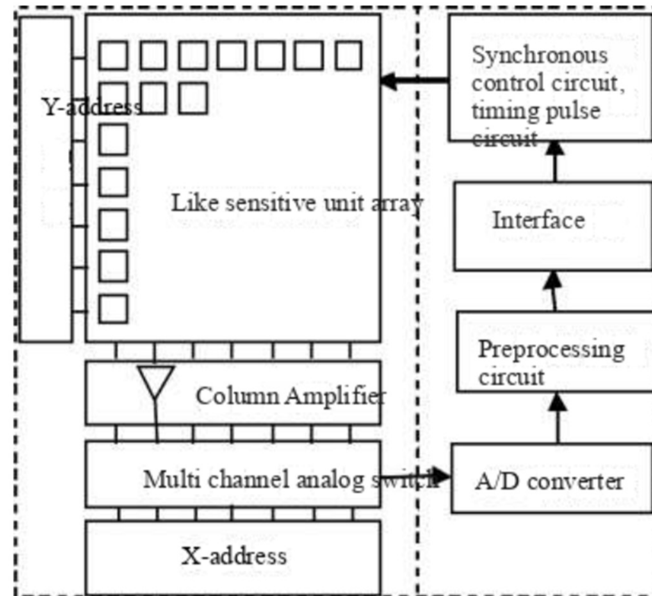

Figure 1. CIS Block Diagram

A CIS is essentially a System-on-Chip that integrates photoelectric conversion, signal processing, and intelligent control. Its core functions include: photoelectric conversion, charge storage and transfer, signal readout and amplification, noise suppression (a key for performance assurance), analog-to-digital conversion, on-chip image processing, high-speed data output, and integration of specific functions.

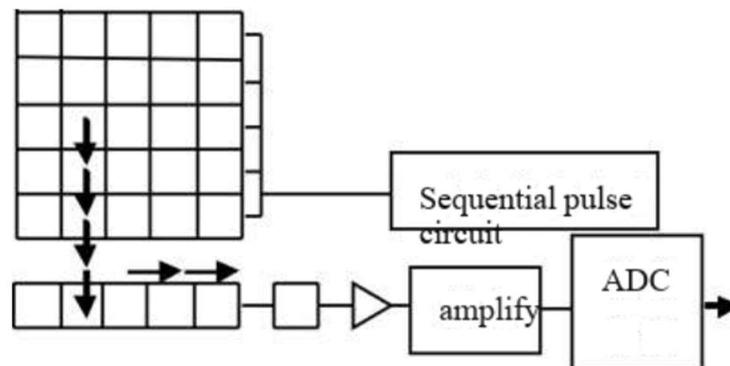

Figure 2. CIS Principle Block Diagram

3. CIS Pixel Performance Parameters

The main performance parameters of a CIS include: quantum efficiency, full-well capacity, readout noise, dark current, dark current non-uniformity, conversion gain, crosstalk, photo-response non-uniformity, linearity, and charge transfer efficiency. This paper will focus on the research and analysis of four of these parameters: conversion gain, dark current, saturation output, and noise.

3.1 Conversion Gain

This refers tothe measure of a single pixel's efficiency in converting photogenerated charge (electrons) into an output voltage.It quantifies the contribution of each photogenerated electron to the output signal voltage. Its physical essence is the capacitance of the charge storage node (usually the floating diffusion). Conversion gain is a critical parameter in the trade-offs of pixel design and system performance, as it affects multiple core performance indicators of an image sensor,such as readout

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noise, full-well capacity, dynamic range, and the quantization precision of the analog-to-digital converter.

3.2 Dark Curren

Dark current is the non-ideal net currentgenerated by thermal excitationin complete darkness,formed by carriersand is unrelated to incident photons. It mainly originates from the following sources:

Generation in the depletion region (primary cause): Electron-hole pairs are generated by lattice vibrations within the depletion region [2].

Surface generation: At the silicon-silicon dioxide ($Si\text{-}SiO_2$) interface,$Si\text{-}SiO_2$a large number of interface states (dangling bonds, defects) exist, which promote carrier generation.

Diffusion current: In the neutral regions adjacent to the depletion region, minority carriers can diffuse to the edge of the depletion region and are then swept away by the electric field, forming a current.

Tunneling current: In regions with very high doping or strong electric fields, tunneling effects can occur, generating additional current. This is becoming increasingly significant in advanced process nodes (small-sized pixels).

Dark current is a key factor limiting the ultimate performance of a CIS, especially in low-light, high-temperature, and long-exposure applications. Its main effects include generating dark current shot noise, occupying full-well capacity, reducing dynamic range, affecting low-light imaging sensitivity, causing image lag, and exacerbating temperature sensitivity.

3.3 Saturation Output

Saturation output refers to the maximum usable, linear signal output level that a single pixel in a CMOS image sensor can produce. It directly corresponds to the pixel's full-well capacity. When photons strike a pixel's photodiode, they generate electron-hole pairs (photogenerated charge). This charge is collected and stored in a physical region within the pixel known as a potential well. This potential well acts like a "charge bucket," and the maximum amount of charge it can hold is the full-well capacity (FWC). The value of FWC depends on the design and manufacturing process of the pixel unit. A larger FWC means that the pixel unit can accommodate more photons, and to a certain extent, it can improve the sensitivity and dynamic range of the sensor, thereby enhancing the signal-to-noise ratio (SNR) of the image[3].

Saturation State: When the incident light intensity increases to a certain point, the rate of photogenerated charge production exceeds the pixel's readout rate or reaches the physical limit of the potential well, and the well becomes full. Any additional charge generated by further incident photons will either spill over (diffuse to adjacent pixels) or be recombined (unable to contribute effectively to the signal). At this point, the pixel's output signal no longer increases linearly with the incident light intensity.

3.4 Noise

This refers to non-ideal signal components, manifesting as random fluctuations or fixed deviations in the output signal. Noise in a CIS is divided into two main categories: random noise and fixed-pattern noise. Random noise includes photon shot noise, dark current shot noise, and readout noise. Fixed-pattern noise includes dark current non-uniformity and photo-response non-uniformity.

4. Analysis of Influencing Factors and Their Principles

4.1 The Effect of Temperature on CIS Pixel Performance

4.1.1 Conversion Gain

It decreases almost linearly with rising temperature (approx. -0.1% to -0.3%/°C).This causes signal amplitude compression, meaning the output voltage produced by the same amount of photogenerated charge is lower, which weakens the signal-to-noise ratio of weak light signals. It also leads to a loss

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of quantization precision, resulting in fewer grayscale levels in the image. The principles by which temperature affects conversion gain are as follows:

(1) Carrier mobility degradation (primary cause). Increased temperature intensifies lattice thermal vibrations, which increases the probability of carrier scattering and reduces mobility.

(2) Threshold voltage drift. An increase in temperature leads to a rise in the intrinsic carrier concentration, causing the threshold voltage VthTHto decrease and, consequently, a drift in the Fermi level.

(3) Floating diffusion capacitance (C_FD)FDexpansion. The capacitance in a CIS is mainly composed of PN junction capacitance and metal capacitance. The built-in potential (Vbi)biand depletion region width (Wd)dof the PN junction capacitance both change with temperature. The dielectric constantεoxof the metal capacitance increases slightly with rising temperature, causing C_FDFDto expand as well. Since CG = q / C_FDFD , the expansion of the floating diffusion capacitance leads to a decrease in conversion gain.

4.1.2 Dark Current

The Impact of Temperature on Dark Current is a Core Factor in CIS Performance Degradation, with the Following Key Aspects:

(1) Exponential growth of dark current: For every 8 to 10°C increase in temperature, dark current doubles. This can cause a dark current that is only 10 to 100 e^-/p/s at room temperature to rise to $10^3$4to $10^4$5e^-/p/s, becoming the dominant noise source.

(2) Increase in dark current shot noise: An increase in temperature leads to higher dark current. According to the formula for dark current shot noise, it is proportional to the square root of the dark current, so it increases as the temperature rises.

4.1.3 Saturation Output / Full-Well Capacity

At high temperatures (above room temperature), FWC typically increases slightly. The bandgap of silicon decreases slightly as temperature rises, leading to a sharp increase in the intrinsic carrier concentration. This allows the depletion region of the photodiode to expand more easily, reducing the depletion capacitance and thus slightly increasing the charge storage capacity.

At low temperatures (below room temperature), FWC may decrease slightly. The bandgap widens, the intrinsic carrier concentration drops, the depletion region contracts, and the depletion capacitance increases, resulting in a slight reduction in storage capacity.

4.1.4 Noise

An increase in temperature leads to an increase in almost all major types of pixel noise:

Dark Current Shot Noise: This is the most significant and fastest-growing noise source. Shot noise originates from the random nature of charge generation events, and its magnitude is proportional to the square root of the dark current. Since dark current grows exponentially with temperature, its shot noise also exhibits an exponential growth trend.

Fixed-Pattern Noise (FPN):

Dark Current Non-Uniformity (DCNU): The absolute difference in dark current between pixelsis significantly amplified as temperature rises. This leads to a substantial increase in FPN.

Photo-Response Non-Uniformity (PRNU): PRNU itself is relatively insensitive to temperature, but at high temperatures, the slight change in conversion gain and the exponential growth of dark current indirectly exacerbate the visual severity of FPN[4].

Thermal Noise: The thermal noise power of resistors in the source follower and readout circuitry is proportional to the absolute temperature. Therefore, its noise voltage amplitude increases with the square root of the temperature.

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4.2 The Effect ofRadiation on CIS Pixel Performance

Radiation environments (such as in space, nuclear facilities, particle accelerators, and medical radiotherapy equipment) can cause significant degradation in the pixel performance of a CIS. These effects primarily arise from the interaction of radiation with the silicon material and device structures, which produces ionization effects and displacement damage (destruction of the crystal lattice). The specific effects of radiation on pixel performance parameters are as follows:

4.2.1 Decrease in Conversion Gain:

CGEffect: Radiation exposure typically leads to a reduction in the pixel's conversion gain. Conversion gain is defined as the efficiency with which a pixel converts collected photogenerated charge into an output voltage.

A decrease means that the same amount of charge produces a smaller signal voltage or digital value. This manifests as a weakening of the overall signal amplitude in the image and a decrease in the signal-to-noise ratio. Especially under low-light conditions, the image will appear darker or require higher gain, and the dynamic range may also be compromised.

4.2.2 Significant Increase in Dark Current:

Effect: This is one of the most significant and pervasive effects of radiation on CIS. Radiation (especially displacement damage effects) causes a dramatic increase in dark current, often by several orders of magnitude[5,6]. This manifests as a large number of randomly distributed "hot pixels" (individual pixels that are abnormally bright), "white spots," or "bright clusters" in the image. Under long exposure, the background brightness of the entire image (the noise floor) increases significantly, and in severe cases, the image is "drowned" in noise. The dark current increase caused by proton irradiation is typically far greater than that from ionization effects at the same dose. Dark current non-uniformity also worsens, leading to increased fixed-pattern noise.

4.2.3 Reduction in Saturation Output:

Effect: The maximum amount of charge that a pixel can store and read out (full-well capacity), or its corresponding maximum output voltage/digital value, decreases[6,7]. This manifests as pixels reaching saturation more easily, causing high-brightness areas in the image (such as strong light sources or reflections) to "spill over" or become "overexposed," resulting in a loss of detail. The upper limit of the dynamic range is compressed. In extreme cases, a pixel may completely lose its photosensitivity.

4.2.4 Overall Increase in Noise:

Dark current shot noise is the primary source of the noise increase. Dark current itself is random, and its shot noise is proportional to the square root of the dark current. A sharp increase in dark current inevitably leads to a substantial rise in its shot noise.

Readout noise. Total ionizing dose (TID) radiation degrades the performance of the source follower transistors within the pixel and the row/column readout circuitry, increasing their 1/f noise and thermal noise. Displacement damage can also introduce additional scattering centers in the source follower channel, increasing thermal noise.

Fixed-pattern noise. Dark current non-uniformity and inter-pixel non-uniformity in conversion gain become more severe after radiation, leading to an increase in FPN. The non-uniformity is exacerbated by the differing responses of pixels to radiation. This manifests as a noticeable increase in overall image noise ("snow"), blurring of details, and severe degradation of image quality, especially in low-light or high-gain scenarios, along with a significant drop in the signal-to-noise ratio.

4.3 The Influence of Pixel Structure on Performance

The pixel structure is the foundation that determines CIS performance. Different designs directly affect core parameters through physical layout and device combinations:

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4.3.1 Conversion Gain Dominated by Floating Diffusion (FD) Node Capacitance

The FD node capacitance is the core of conversion gain (CG ∝ 1/C_FD).CG = q / C_FD Structurally, a smaller FD area and lower parasitic capacitance result in a higher CG.

SharedFDvs. Unshared Structures: In a 4T4Tpixel, the transfer gate is directly connected to theFDFD, resulting in a relativelyCGhigh CG. In contrast, a 3T3T pixel, lacking an independentFDFD and with the reset transistor sharing a node with the source follower, has large parasitic capacitance and thus aCGlower CG.

BSI Advantage: BSI eliminates metal wiring obstruction, allowing for a larger photo diode (PD) area, but high CG can be maintained by optimizing and shrinking the FD

4.3.2 Dark Current

Shallow Trench Isolation (STI) Interface: efects at the STI sidewall and silicon interface are a major source of dark current. Structures with a high pixel boundary-to-area ratio (i.e., small pixels) have higher dark current.

Photodiode (PD) Design:

Pinned PD: A surface p+ layer creates hole accumulation, suppressing current generation from interface states and reducing dark current by a factor of 10-100.

Buried PD: Moves the depletion region away from the surface, reducing interface effects.

BSIBSI Structure: Eliminates front-side metal/and polysilicon obstruction, but requires managing Si-SiO_2-interface defects, relying on passivation processes.

Optimized BSI structures can reduce dark current to <1 e^-/s/pixel,0.1-1 e^-/pix/s（25°Cwhereas traditional designs can be as high as 10-100 e^-/s/pixel.100 e^-/pix/s

4.3.3 Saturation Output and Full-Well Capacity (FWC)

PD Size and Depth: The PD area and depletion region volume directly determine charge storage capacity. BSI, lacking metal obstruction, allows for an increased PD area, boosting FWC.

Voltage and Design Constraints:

Global Shutter (GS) and Rolling Shutter (RS): GS pixels, with dual storage nodes (PD + memory node), occupy more area, so their FWC is typically lower than that of RS pixels.

High-Bias Design: A deep-depletion PD can expand the depletion region, but breakdown must be prevented.

Process Optimization:

Dual Conversion Gain (DCG): High-gain mode offers high CG but low FWC; low-gain mode increases FWC by enlarging the FD capacitance.

Modern BSI and CIS FWC can reach 20,000-40,000 e^-, while Front-Side Illumination (FSI) is around 10,000-20,000 e^-.

4.3.4 Noise

Readout Noise:

kTC Noise: A smaller Floating Diffusion (FD) capacitance (C_FD) results in lower kTC noise. The independent FD in a 4T pixel allows for C_FD optimization, thereby reducing kTC noise.

Source Follower: A shared Source Follower (SF) architecture (e.g., shared by multiple pixels) reduces the layout area but increases the load capacitance, which can lead to higher thermal noise[8].

Fixed-Pattern Noise (FPN):

Symmetrical Layout: Symmetrical layouts with matched transfer gates and reset transistors reduce variations in threshold voltage, thus improving FPN.

Shared ADC: Column-parallel ADC reduce circuit mismatches, but the long-distance transmission of analog signals can introduce crosstalk.

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Shot Noise: Non-uniformity in dark current is positively correlated with the pixel's perimeter-to-area ratio; smaller pixels are more sensitive to this effect.

The readout noise of pixels in advanced BSI+4T processes can be reduced to [value] 1-2 e^-, while 3T pixels in [older processes] are often higher than [value].10 e^-

4.4 Impact of Manufacturing Processes on CIS Pixel Performance

4.4.1 Conversion Gain (CG)

A higher n+ doping concentration at the Floating Diffusion node increases depletion capacitance, which in turn lowers the Conversion Gain. Ultra-shallow junction processes can reduce this capacitance, thereby boosting CG.

Gate Oxide Thickness: The thickness of the FD reset transistor's gate oxide affects parasitic capacitance. A thin gate oxide (less than 5nm) reduces capacitance but increases the risk of quantum tunneling noise.

Metal Interconnects: High-density metal routing around the FD increases parasitic capacitance, which can reduce CG by 10-20%.

The CG in an [advanced]40nm BSIprocessCGcan reach [value]200 μV/e^-, while90nm FSIfor an [older] process, it is only [value].50-80 μV/e^-

4.4.2 Dark Current

Hydrogen Annealing: Hydrogen passivation of the silicon interface repairs dangling bonds, lowering the interface state density and reducing dark current by a factor of 5-10.

Low-Temperature Processing: Reduces impurity diffusion caused by high-temperature annealing, suppressing the formation of defects.

Doping Uniformity: Deviations in the ion implantation angle can causePDnon-uniform doping at the device edges, increasing edge leakage current.

Shallow Trench Isolation (STI)Process: High-energy plasma etching can damage the silicon lattice. If this damage is not annealed, dark current can increase by a factor of3-5[value].

At 25°C, the dark current for a high-quality process can be as low as<0.1 e^-/p/[value] (for scientific-grade CIS), while for consumer-grade CIS, it is typically around [value].1-5 e^-/p/s

4.4.3 Saturation Output and Full Well Capacity (FWC)

Deep Implantation: High-energy phosphorus/arsenic implantation creates a deep depletion region (3-5μm), increasing FWC by 30-50%.

Graded Doping: A graded doping profile extends the depletion region width (W), and FWC is proportional to W (FWC $\propto$ W).[2]

Chip Thickness:BSIIn [BSI] processes, the silicon wafer is thinned to [thickness]2-5μm, which limits the vertical charge capacity, resulting in a lower FWC than thick-silicon sensors.

Microlens Efficiency: When the light-gathering efficiency of the microlens>90% is [high], the effective number of photogenerated electrons increases, which indirectly boosts the saturation signal.

The FWC of a deep-depletion processFSIand [its saturation level] CIS，FWC can reach [value]40,000 e^-, BSI, while [BSI sensors], due to thickness constraints, are typically [lower].<30,000 e^-.

4.4.4 Noise

kTCkTC Noise:FDThe FD node capacitance, C_FD determined by doping and layout, directly impacts kTC noise. C_FD<1 fF When [capacitance is low]kTC, this noise [is low]<4e^-.

1/fFlicker (1/f) Noise:

Gate Oxide Quality: Thermally grown oxideSiO_2has a lower interface state density than deposited oxide,1/freducing 1/f noise by a factor of2-3[value].

Transistor Sizing: Using a larger source follower transistor reduces the magnitude of 1/f noise.

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28nmThe readout noise in an [advanced] process can be reduced to [value]0.8 e^-(CDS(after [post-processing]), 65nm while in an [older] process, it is approximately [value].2-3 e^- Future 3D stacking processes will further separate the photo diode and circuit layers, overcoming the traditional trade-off between area and noise.

4.5 Potential Optimization Strategies

Based on the previous research content of this article,the following are potential methods for improving CIS pixel performance,categorized by four key factors: temperature, radiation, pixel structure, and manufacturing process.

4.5.1 Optimizing for Temperature Effects

Dark Current Suppression

Deep Cooling Technology: Using a thermoelectric cooler (TEC) to lower the chip temperature to below-40°C[value] can reduce dark current to <0.01 e^-/p/s[a very low level] (suitable for astronomical/and scientific imaging).

On-Chip Temperature Compensation: An integrated temperature sensor can be used to generate a real-time dark frame correction map to eliminate hot pixels.

Conversion Gain Stability

Low Temperature-Coefficient Capacitors: Replacing PN junction capacitors with Metal-Insulator-Metal (MIM) capacitors to suppress temperature-induced drift.

Adaptive Biasing: Dynamically adjusting the source follower's bias voltage to compensate for threshold voltage drift.

Noise Control

Dual-Gain Pixel Design: At high temperatures, switch to a low-gain mode to reduce dark shot noise; at low temperatures, activate a high-gain mode to improve low-light sensitivity.

4.5.2 Hardening Methods Against Radiation Damage

Design for Tolerance to Ionizing Effects

Enclosed-Layout Transistors (ELTs): Eliminate gate oxide edge effects, enabling tolerance to a total ionizing dose (TID) of >100 krad(Si).

Buried-Channel Transfer Gates: The charge transfer path is located away from theSiO_2Si-SiO2 interface, reducing the probability of trapping at interface states.

Design for Tolerance to Displacement Damage

Silicon Carbide (SiC) Substrate: With a bond energy three times higher (4.6 eV), SiC improves resistance to proton-induced displacement damage by a factor of 10.

Defect Self-Healing: A phosphorus-doped "gettering zone" can be built into the photodiode's depletion region to capture vacancy defects.

4.5.3 Innovations in Pixel Structure

Balancing High Dynamic Range (HDR) and Sensitivity

Vertically Stacked Photodiodes:BSI+3DUsing [a specific] integration technology, the upper PD layer collects short-wavelength light, while the lower PD layer collects long-wavelength light. This increases quantum efficiency>80%across the full spectrum,FWCboosting it to [value].60,000 e^-

Microlens Light-Field Modulation: An aspherical microlens array focuses obliquely incident light onto the center of the photo diode, reducing edge leakage current.

Global Shutter Optimization

Charge-Domain Storage: Using a deep, depleted well for in-pixel storage instead of a metal node, achieving a full well capacity loss of <10%.

Noise Suppression

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Shared Floating Diffusion: Some High-precision pixel sharing FD, reducing capacitance and suppressing noise[8].

4.5.4 Breakthroughs in Manufacturing Processes

Atomic-Level Control of Interface Defects

Atomic Layer Passivation: A passivation layer is deposited Al_2O_3/HfO_2 and stacked on the silicon interface, achieving a fixed charge density,$>5\times10^{12}$ cm^{-2} thereby reducing dark current to0.05 e^-/p/s(60°C).

Low-Temperature Wafer Bonding: Direct Silicon Bonding (DSB) below 300°C eliminates lattice defects caused by thermal stress.

Innovations in Doping Engineering

Plasma Immersion Ion Implantation: Achieves PD vertically ultra-uniform doping, with a concentration gradient<5%/nm），FWC improved to 50,000 e^-

Laser Annealing Activation: Nanosecond laser selectively injects energy, reducing impurity diffusion and driving the temperature coefficient of capacitance (TCC) of the Floating Diffusion (FD) node towards zero.

3D Integration Processes

Copper-to-Copper (Cu-Cu) Hybrid Bonding: The vertical interconnect pitch between the photodiode layer and the logic layer is ≤1μm, supporting in-pixel integration ADC and reducing readout noise to 0.3 e^-approximately

5. Conclusion

The breakthroughs in the performance boundaries of CMOS Image Sensor (CIS) pixels are the result of the synergistic evolution of materials physics, device design, and process technology. As the "intelligent eye" of the machine vision era, its performance directly determines the frontiers of breakthroughs in multiple advanced fields. As pixel sizes approach their physical limits and application scenarios become more extreme (e.g., high temperature, high radiation), traditional structures face three major bottlenecks: runaway dark current, a shrinking dynamic range, and the accumulation of radiation damage. Current CIS technology exhibits a polarization: For consumer-grade applications,BSIstacking technologies have pushed pixel miniaturization down to 0.8μm sub-micron levels, but high-temperature dark current (>100 e^-/s) and dynamic range (<100 dB) constrain low-light performance. In specialized fields, radiation-hardened CIS relies on bulky cooling systems and redundant designs, resulting in high power consumption and high cost. The core conflict lies in the "impossible triangle" of performance, reliability, and cost, a challenge that urgently needs to be overcome through synergistic innovation in materials, structures, and processes. This study, based on a review of existing literature, analyzes the influence of four factors-temperature, radiation, pixel structure, and manufacturing processes-to reveal the mechanisms affecting pixels under multi-stress coupling. The aim is to provide a theoretically viable reference framework for designing highly reliable and versatile CIS. In the future, CIS technology will inevitably trend towards higher sensitivity, larger pixel counts, higher frame rates, wider dynamic range, lower noise with superior image quality, stronger radiation hardness, lower power consumption, and more compact sizes. As the market increasingly moves toward low-cost, lightweight products, CMOS technology stands out as an excellent choice. With the continued development and refinement of image sensing technology, its future prospects are immeasurable.

References

[1] Lin Y. (2005) CIS Tending to Replace CCD. Electronic Technology, (09): 15-18.

[2] Simon M. Sze & Kwok K. Ng (2006) Physics of Semiconductor Devices (3rd ed.). Xi'an Jiaotong University Press, Wiley.

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[3] Chen J., Guo J., Zhong X., Gu X., Yu Z. (2025) Research Progress on Noise Suppression for CIS. Electronics & Packaging, 25(06): 84-96.

[4] Joseph, D. and Collins, S. (2009) "Temperature Dependence of Fixed Pattern Noise in Logarithmic CMOS Image Sensors," in IEEE Transactions on Instrumentation and Measurement, 58(8): 2503-2511.

[5] Zheng R., Liu C., Liu H., Hui X. (2018) Prediction Method for Dark Current Amplitude Distribution of CMOS Image Sensors in Radiation Environment. Microelectronics & Computer, 35(04): 144-148.

[6] Peng Z., Bai H., Liu F., et al. (2025) Influence of Proton Cumulative Irradiation Effects on CIS Saturation Output. Acta Physica Sinica, 74(02): 102-113.

[7] Mao Z. (2022) Research on CIS Imaging Performance Testing Technology. University of Chinese Academy of Sciences (Changchun Institute of Optics, Fine Mechanics and Physics, Chinese Academy of Sciences).

[8] Chen J., Guo J., Zhong X., Gu X., Yu Z. (2025) Research Progress on Noise Suppression for CMOS Image Sensors. Electronics and Packaging, 25(06): 84-96.