

# An Optimization Method for DC Side Voltage Balance Control of HC-SVG based on Delay Signal Cancellation

Xiaofan Zhao<sup>1,2</sup>, Shaotong Du<sup>1,\*</sup>

<sup>1</sup> School of Electrical Engineering and Automatic, Henan Polytechnic University, Jiaozuo 454000, China

<sup>2</sup> State Grid Henan Electric Power Company Anyang Power Supply Company, Anyang 455000, China

---

## Abstract

**Abstract:** The integration of NPC high-voltage power units into HC-SVG systems introduces high harmonics in the DC capacitor voltage of the CHB unit and NPC DC bus side capacitor voltage, impacting device compensation performance. This study presents a comprehensive analysis of the DC side capacitor voltages of the CHB and NPC units, identifying and assessing their harmonic components. Subsequently, a filter scheme is devised utilizing the delay-cancellation method based on the triangle vector principle to optimize the DC voltage control of the CHB and NPC units. A simulation platform is constructed to validate the proposed theoretical framework. Results demonstrate that the optimized control strategy markedly enhances the compensation capabilities of HC-SVG systems, leading to a notable reduction in total harmonic distortion in both output voltage and compensation current under identical operational conditions, thereby enhancing the compensation performance of HC-SVG systems.

## Keywords

Hybrid Cascaded SVG; Harmonics; Fast Delay Signal Cancellation; Vector Triangle; Filter.

---

## 1. Introduction

Hybrid cascaded SVG is an advanced power electronic device. Its topology is usually composed of multiple cascaded modules to achieve high voltage output and low harmonic distortion<sup>[1]</sup>. Each module can be an H-bridge inverter or a three-level inverter. Hybrid cascade topology can reduce the number of power cells required, reduce switching losses and improve device power density effectively, which is a research hotspot of cascade converter.

It is determined that when the DC voltage utilization ratio matches that of the conventional H-bridge cascaded Static Var Generator (SVG), the DC voltage of the high voltage unit in Hybrid Cascaded SVG (HC-SVG) employing Neutral Point Clamped (NPC) and H-bridge topologies can be elevated to 1.3 times the modulation voltage amplitude in references [2]-[4]. Nonetheless, the integration of a high voltage unit into the hybrid cascade system will elevate the harmonic content of the DC side capacitance of the Capacitor-Clamped H-Bridge (CHB), consequently posing a significant threat to the device's stability.

Fast Delayed Signal Cancellation (FDSC) based on vector triangle principle is introduced in references [5]-[6]. The core idea is that the vector triangle is formed by three equal interval sampling, and the sampling values of the current sampling period and the delayed sampling period are used. According to the vector composition rule, the vector sum of two sampled voltages is equal in magnitude and opposite in direction to the harmonics of another sampled voltage, thus achieving

efficient harmonic cancellation, which has become a hot spot in harmonic analysis and extraction in the current electrical engineering field.

Based on the delay signal cancellation method, this paper designs a filter to eliminate harmonics in the DC side capacitor voltage of each unit. Finally, the DC side optimization control scheme of HC-SVG is constructed, and the main circuit parameters of 6kV/3Mvar HC-SVG are selected. The effectiveness of HC-SVG is verified by simulation.

## 2. HC-SVG Topology

HC-SVG is composed of NPC high voltage power unit and CHB low voltage power unit.

As shown in Figure 1,  $i_{sa}$ ,  $i_{sb}$ , and  $i_{sc}$  respectively represent three-phase current at grid side;  $u_{sc}$ ,  $u_{sa}$ ,  $u_{sb}$  refer to voltage of common connection point relative to neutral point N;  $L_s$  represents equivalent impedance of grid;  $i_{fa}$ ,  $i_{fb}$ , and  $i_{fc}$  are three-phase current at load end;  $i_a$ ,  $i_b$ , and  $i_c$  are three-phase compensation current provided by HC-SVG; equivalent inductance value of filter reactor is represented by  $L_{eq}$ .

The voltages of the DC side capacitors of the CHB power unit in phase A are denoted as  $u_{cha1}$ ,  $u_{cha2}$ , and  $u_{chan}$ . The variables  $u_{chk}$  ( $k=a,b,c$ ) represent the three-phase output voltages of the CHB power unit. The parameter  $C_h$  signifies the nominal capacity of the DC side capacitor of the CHB. The switching elements  $V_{a1}$  to  $V_{a4}$  in the NPC power unit are high-voltage IGBT devices. The variables  $u_{npca}$ ,  $u_{npcb}$ , and  $u_{npcc}$  represent the three-phase output voltages of the NPC three-level power unit with respect to the reference point O. The variable  $u_{dc}$  signifies the total voltage on the DC side of the NPC unit, while  $u_{dc1}$  and  $u_{dc2}$  denote the voltages across the two independent capacitors on the DC side of the NPC unit.  $C_n$  represents the rated capacity of the DC side capacitor of the NPC unit.

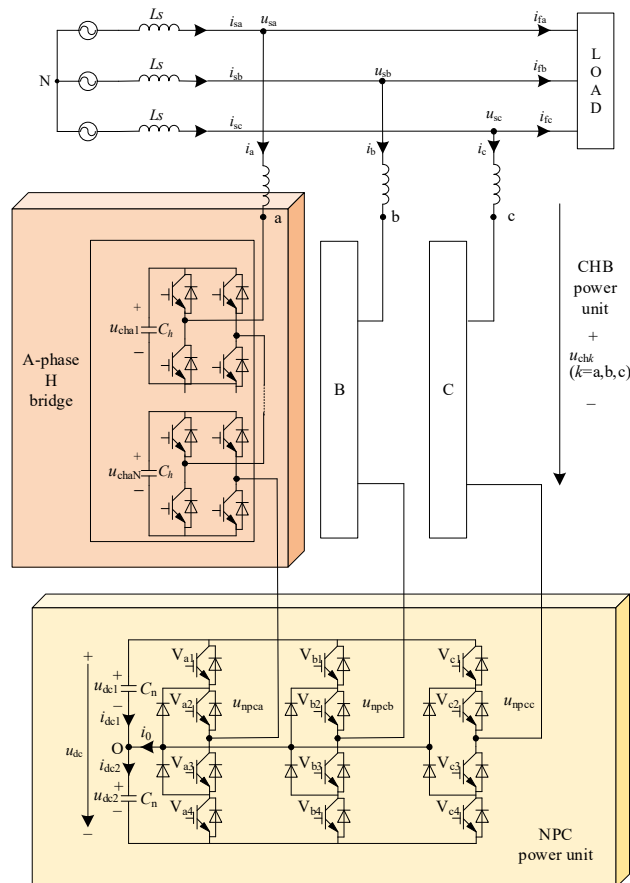


Figure 1. HC-SVG topology diagram

CHB power unit adopts carrier phase shift modulation, NPC three-level power unit adopts nearest level approximation modulation method. Let A phase modulation reference voltage in HC-SVG be

$$u_a^* = U_m \sin(\omega t) \tag{1}$$

Where  $U_m$  is the amplitude of HC-SVG modulation reference voltage;  $\omega$  is the fundamental angular frequency of the grid;  $t$  is time.

Then the CHB power unit modulation reference voltage expression is

$$u_{cha}^* = u_a^* - S_{npca} \times \frac{u_{dc}}{2} \tag{2}$$

Figure 2 visually illustrates the modulation reference voltage for each cell. Specifically,  $u_a^*$  represents the A-phase modulation reference voltage waveform in HC-SVG, with  $\alpha$  denoting the phase angle ranging from 0 to  $u_{dc}/2$  corresponding to  $unpca$ . Here,  $u_{npca}$  stands for the waveform of the output voltage of the NPC power unit A phase, while  $S_{npca}$  signifies the switching function of the NPC three-level power unit A phase.

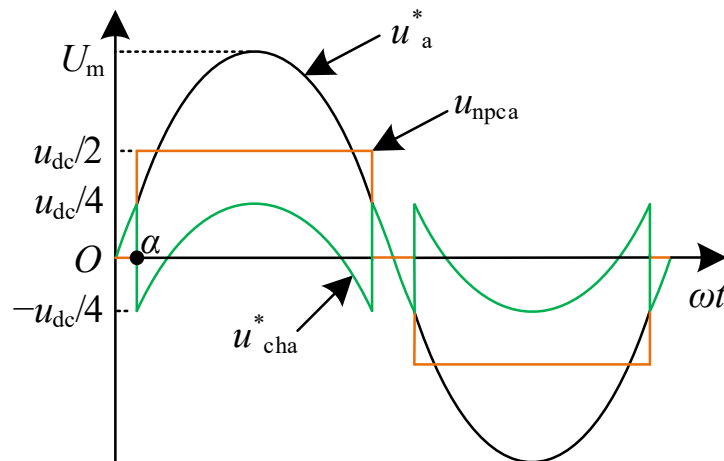


Figure 2. HC-SVG topology diagram

### 3. DC Side Capacitor Voltage Harmonic Analysis

Compared with traditional H-bridge, HC-SVG contains more harmonic components than traditional H-bridge due to NPC high-voltage unit, not only the second harmonic component. This problem will affect the performance and accuracy of DC voltage balance control link, and affect the output waveform of HC-SVG, reducing its compensation characteristics. This section will analyze this problem. Through Fourier analysis of CHB and NPC unit modulation voltage, the circuit model is established, and the time domain expression of corresponding capacitor voltage is obtained to further determine the harmonic condition of DC side capacitor voltage.

#### 3.1 Harmonic Analysis of CHB Unit Capacitance Voltage

First, it can be seen from Figure 2 that the CHB cell modulation voltage waveform can be expressed as follows

$$u_{cha}^*(t) = \begin{cases} \frac{3}{4}u_{dc} \sin \omega t - \frac{1}{2}u_{dc} & t \in \left[ \frac{\alpha T}{2\pi}, \frac{(\pi-\alpha)T}{2\pi} \right] \\ \frac{3}{4}u_{dc} \sin \omega t & t \in \left[ 0, \frac{\alpha T}{2\pi} \right) \cup \left( \frac{(\pi-\alpha)T}{2\pi}, \frac{(\pi+\alpha)T}{2\pi} \right) \cup \left( \frac{(2\pi-\alpha)T}{2\pi}, T \right] \\ \frac{3}{4}u_{dc} \sin \omega t + \frac{1}{2}u_{dc} & t \in \left[ \frac{(\pi+\alpha)T}{2\pi}, \frac{(2\pi-\alpha)T}{2\pi} \right] \end{cases} \quad (3)$$

Fourier analysis of modulation voltage of CHB power unit is carried out, and its Fourier series expression is

$$\begin{cases} u_{cha}^*(t) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty} [a_n \cos(n\omega t) + b_n \sin(n\omega t)] \\ a_n = \frac{2}{T} \int_0^T u_{cha}^*(t) \cos(n\omega t) dt \\ b_n = \frac{2}{T} \int_0^T u_{cha}^*(t) \sin(n\omega t) dt \end{cases} \quad (4)$$

Since  $u_{cha}^*(t)$  is an odd function and passes through the origin, the DC component coefficients  $a_0$  and  $a_n$  are both zero.

The calculated coefficient  $b_n$  is

$$b_n = \begin{cases} \frac{3}{4}u_{dc} & n = 1 \\ 0 & n \text{ is an even number} \\ -\frac{2u_{dc}}{n\pi} \cos(n\alpha) & n \text{ is an odd number and } n \neq 1 \end{cases} \quad (5)$$

CHB three-level power unit modulation voltage can be obtained

$$\begin{aligned} u_{cha}^*(t) &= \frac{3}{4}u_{dc} \sin \omega t - \frac{2u_{dc}}{\pi} \cdot \frac{\cos(3\alpha)}{3} \sin(3\omega t) - \frac{2u_{dc}}{\pi} \cdot \frac{\cos(5\alpha)}{5} \sin(5\omega t) - \dots \\ &= \frac{3}{4}u_{dc} \sin \omega t - \frac{2u_{dc}}{\pi} \sum_{k=1}^{\infty} \frac{\cos((2k+1)\alpha)}{2k+1} \sin((2k+1)\omega t) \end{aligned} \quad (6)$$

Assuming that the DC side capacitance of each H-bridge module in CHB unit has the same working condition, there is

$$U_{c_{kn}} = U_c \quad n = 1, 2, \dots, N \quad (7)$$

Phase A is selected for analysis. Through modeling analysis process, the behavior describing DC side capacitance of single sub-module in CHB unit can be obtained, that is

$$C_h \frac{du_{ch}(t)}{dt} = s_{cha}(t) i_a(t) \quad (8)$$

Where  $u_{ch}$  is the actual voltage of a single DC side capacitor of CHB power unit, and  $S_{cha}$  is the switching function of CHB power unit submodule.

The switching function  $S_{cha}$  obtained from equation (1)(2) can be expressed as

$$s_{cha}(t) = \frac{u_{cha}^*(t)}{NU_c} \quad (9)$$

The three-phase compensation current of HC - SVG is set as

$$\begin{cases} i_a = I_m \sin(\omega t + \varphi) \\ i_b = I_m \sin\left(\omega t + \varphi - \frac{2\pi}{3}\right) \\ i_c = I_m \sin\left(\omega t + \varphi + \frac{2\pi}{3}\right) \end{cases} \quad (10)$$

Where:  $I_m$  is the amplitude of HC-SVG rated current,  $\varphi$  is the angle of compensation current leading compensation voltage,  $\omega$  is the fundamental frequency of power grid,  $t$  is time.

To simplify the analysis, assuming that HC-SVG outputs only reactive power, the phase A compensation current in HC-SVG devices can be expressed as

$$i_a = I_m \sin(\omega t \pm 90^\circ) = \pm I_m \cos(\omega t) \quad (11)$$

In this paper, the upper symbol denotes a capacitive compensation condition, while the lower symbol signifies an inductive compensation condition.

From equation (8)(9)(11), we can obtain

$$C_h \frac{du_{ch}(t)}{dt} = \frac{u_{cha}^*(t)}{NU_c} i_a(t) \quad (12)$$

Simplifying the above expression and further integrating the left and right sides of the expression yields the following expression, we can obtain

$$u_{ch}(t) = \frac{1}{C_h NU_c} \int u_{cha}^*(t) i_a(t) dt \quad (13)$$

Substituting equation (6) into (13) yields

$$u_{ch}(t) = \frac{1}{C_h N U_c} \int u_{cha}^*(t) i_a(t) dt \tag{14}$$

$$= \pm \frac{I_m}{C_h N U_c} \int \left[ \left( \frac{3}{4} u_{dc} \sin \omega t - \frac{2u_{dc}}{\pi} \sum_{k=1}^{\infty} \frac{1}{2k+1} \cos((2k+1)\alpha) \sin((2k+1)\omega t) \right) \right] \cdot \cos(\omega t) dt$$

To simplify the expression, define the constant  $F_1 = \pm I_m / C_h N U_c$  and expand the terms to obtain

$$u_{ch}(t) = \frac{3u_{dc}}{4} F_1 \int \sin \omega t \cdot \cos(\omega t) dt - \frac{2u_{dc}}{\pi} F_1 \int \sum_{k=1}^{\infty} \frac{\cos((2k+1)\alpha)}{2k+1} \sin((2k+1)\omega t) \cdot \cos(\omega t) dt \tag{15}$$

$$= \bar{u}_1 - \frac{3u_{dc}}{16\omega} F_1 \cos(2\omega t) + \frac{u_{dc}}{\pi} F_1 \sum_{k=1}^{\infty} \frac{\cos((2k+1)\alpha)}{2k+1} \left[ \frac{\cos((2k+2)\omega t)}{(2k+2)\omega} + \frac{\cos(2k\omega t)}{2k\omega} \right]$$

In the formula:  $u_1$  is DC component of DC side capacitance voltage of CHB unit.

Equation (15) reveals that the CHB capacitance voltage comprises not only the conventional second harmonic component but also a series of even harmonic components. The amplitude of each harmonic content is proportional to the parameter k, whereby higher values of k correspond to diminished amplitudes.

To sum up, in addition to the traditional second harmonic component, the harmonic components in the DC side voltage of CHB unit are mainly even harmonic components of low order (4th, 6th, 8th).

### 3.2 Harmonic Analysis of Capacitance Voltage on DC Side of NPC Unit

It can be seen in Figure 2, NPC three-level power unit modulation voltage can be expressed as

$$u_{npca}^*(t) = \begin{cases} \frac{u_{dc}}{2} & t \in \left[ \frac{\alpha T}{2\pi}, \frac{(\pi - \alpha) T}{2\pi} \right] \\ 0 & t \in \left[ 0, \frac{\alpha T}{2\pi} \right) \cup \left( \frac{(\pi - \alpha) T}{2\pi}, \frac{(\pi + \alpha) T}{2\pi} \right) \cup \left( \frac{(2\pi - \alpha) T}{2\pi}, T \right] \\ -\frac{u_{dc}}{2} & t \in \left[ \frac{(\pi + \alpha) T}{2\pi}, \frac{(2\pi - \alpha) T}{2\pi} \right] \end{cases} \tag{16}$$

The expression is obtained by performing Fourier analysis on the modulation voltage of the NPC three-level power unit.

$$\begin{cases} u_{npca}^*(t) = \frac{1}{2} a_0 + \sum_{n=1}^{\infty} [a_n \cos(n\omega t) + b_n \sin(n\omega t)] \\ a_n = \frac{2}{T} \int_0^T u_{npca}^*(t) \cos(n\omega t) dt \\ b_n = \frac{2}{T} \int_0^T u_{npca}^*(t) \sin(n\omega t) dt \end{cases} \tag{17}$$

Since  $u_{npca}^*(t)$  is an odd function and passes through the origin, the DC component coefficients  $a_0$  and  $a_n$  are both zero.

The calculated coefficient  $b_n$  is

$$b_n = \begin{cases} \frac{2u_{dc}}{n\pi} \cos(n\alpha) & n \text{ is an odd number} \\ 0 & n \text{ is an even number} \end{cases} \quad (18)$$

The modulation voltage of NPC unit can be obtained as

$$\begin{aligned} u_{npca}^*(t) &= \frac{2u_{dc}}{\pi} \left[ \cos \alpha \sin(\omega t) + \frac{\cos(3\alpha)}{3} \sin(3\omega t) + \frac{\cos(5\alpha)}{5} \sin(5\omega t) + \dots \right] \\ &= \frac{2u_{dc}}{\pi} \sum_{k=0}^{\infty} \frac{1}{2k+1} \cos((2k+1)\alpha) \sin((2k+1)\omega t) \end{aligned} \quad (19)$$

Because NPC side three phases share two capacitors, each capacitor is subject to the current fluctuations of all three phases and cannot be examined in isolation. Nevertheless, considering the symmetry in the power system, phase A can be selected to analyze the waveform expression of a capacitor voltage of NPC unit. By conducting modeling and analysis in the initial subsection, an expression characterizing the behavior of the DC side capacitor in one phase of the NPC unit can be derived as follows:

$$C_n \frac{du_{cn}(t)}{dt} = S_{npca}(t) i_a(t) \quad (20)$$

Where  $u_{cn}$  is the actual voltage of DC side capacitance of A phase NPC unit, and  $S_{npca}$  is the switching function of NPC unit sub-module.

By modeling phase A of NPC unit, it can be obtained that

$$C_n \frac{du_{cn}(t)}{dt} = \frac{u_{npca}^*(t)}{\frac{1}{2}u_{dc}} i_a(t) = \frac{2u_{npca}^*(t)}{u_{dc}} i_a(t) \quad (21)$$

By simplifying the aforementioned expression and further integrating both sides, the following formula is yielded.

$$u_{cn}(t) = \frac{2}{u_{dc} C_n} \int u_{npca}^*(t) i_a(t) dt \quad (22)$$

Substituting equation (19) into (22) yields

$$u_{cn}(t) = \frac{2}{u_{dc} C_n} \int u_{npca}^*(t) i_a(t) dt = \pm \frac{4I_m}{\pi C_n} \int \left[ \sum_{k=0}^{\infty} \frac{\cos((2k+1)\alpha)}{2k+1} \sin((2k+1)\omega t) \right] \cdot \cos(\omega t) dt \quad (23)$$

To simplify the expression, define the constant  $F_2 = \pm 4I_m / \pi C_n$  and expand the terms to obtain

$$\begin{aligned} u_{cn}(t) &= F_2 \int \left[ \frac{2u_{dc}}{\pi} \sum_{k=0}^{\infty} \frac{\cos((2k+1)\alpha)}{2k+1} \sin((2k+1)\omega t) \right] \cdot \cos(\omega t) dt \\ &= \bar{u}_2 - \frac{F_2}{2} \sum_{k=0}^{\infty} \frac{\cos((2k+1)\alpha)}{2k+1} \left[ \frac{\cos((2k+2)\omega t)}{(2k+2)\omega} + \frac{\cos(2k\omega t)}{2k\omega} \right] \end{aligned} \quad (24)$$

In the formula:  $u_2$  is DC component of DC side capacitance voltage of NPC unit.

As revealed by Equation (24), the harmonic constituents in the DC-side voltage of the NPC unit are primarily low-order even harmonics (2nd, 4th, 6th, 8th orders).

#### 4. Design of Delay Signal Cancellation Filtering Method based on Vector Triangle Principle

To address the phenomenon of low-order even harmonics in the DC-side voltage identified in the previous subsection, this section proposes a fast delayed-signal cancellation filtering method based on the vector triangle principle.

##### 4.1 Principle of Fast Delay Signal Cancellation

The time-domain expression for FDSC can be expressed as follows:

$$FDSC(f, d)[\bar{u}(t)] = u(t) + u\left(t - \frac{2T}{d}\right) - u\left(t - \frac{T}{d}\right) \quad (25)$$

Where:  $T$  is the fundamental wave period;  $d$  is the delay coefficient;  $f$  is the filter coefficient.

Applying Laplace transform to the preceding equation yields the s-domain transfer function of FDSC as:

$$FDSC(f, d)[s] = 1 + e^{-\frac{2Ts}{d}} - fe^{-\frac{Ts}{d}} \quad (26)$$

Substituting  $s = j\omega_1$  into equation (26) yields

$$FDSC(f, d)[s] = 1 + e^{-j\frac{2\pi h}{d}} - fe^{-j\frac{2\pi h}{d}} \quad (27)$$

The frequency corresponding to the fundamental voltage is denoted as  $\omega_1$ , which  $h=1$  aligns with the fundamental voltage. By defining, the aforementioned formula can be simplified to derive:

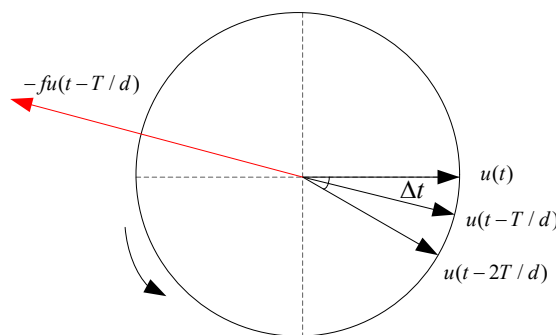
$$\begin{aligned}
 \text{FDSC}(f, d)[s] &= 1 + e^{-2\sigma j} - fe^{-\sigma j} \\
 &= \cos \sigma(2 \cos \sigma - f) - j \sin \sigma(2 \cos \sigma - f) \\
 &= (2 \cos \sigma - f)e^{-\sigma j}
 \end{aligned}
 \tag{28}$$

The final expression for the frequency response characteristics of the FDSC amplitude and phase is

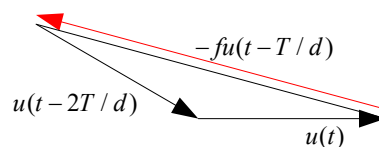
$$\text{FDSC}(f, d)[s] = (2 \cos \frac{2h\pi}{d} - f)e^{-j\frac{2h\pi}{d}}
 \tag{29}$$

From Equation (29), it is evident that after filtering with FDSC(f,d), the amplitude of the h-th voltage harmonic is reduced to  $(2\cos(2h\pi/d) - f)$  times its original value, accompanied by a phase shift of  $-2h\pi/d$ . Furthermore, when the harmonic order h and coefficients f, d satisfy condition  $2\cos(2h\pi/d) - f = 0$ , this corresponds to the cancellation of harmonics at specific frequencies.

Figure 3 illustrates the concept of rapid signal cancellation utilizing vector triangles. In Figure 3(a), three equidistant samples are depicted, with representing the voltage vector at the present time, and denoting the sampled voltage vectors at two specific sampling instances in the past. By appropriately choosing, a vector triangle can be formed using these three voltage vectors for various harmonic orders, ensuring that the triangle fulfills the criterion:  $u(t) + u(t-2T/d) = f \times u(t-T/d)$ , as depicted in Figure 3(b).



(a) Schematic diagram of three-stage equal interval sampling



(b) Vector Triangle Diagram

Figure 3. Principle of fast signal cancellation based on vector triangles

#### 4.2 Design of Delay Signal Cancellation Filter Method Based on Vector Triangle Principle

Four FDSC operators are cascaded to eliminate even-order harmonic components. The filter module design is illustrated in Figure 3. By setting the delay coefficient to 50, the total filter delay can be determined  $\Delta 4T/25$ . This selection involves removing filter coefficients in the filter operator module corresponding to the 2nd, 4th, 6th, and 8th harmonics.

Regarding the DC capacitor voltage, the cascaded filter impacts its DC output amplitude, necessitating amplitude reduction. The amplitude correction coefficient for the DC voltage component is

$$r_0 = \frac{1}{2 \cos \frac{2h_0\pi}{d} - f_h} = \frac{1}{2 - f_h} \quad (30)$$

Then there are amplitude correction coefficients  $h=2$  in the  $r_2=1/2(1-\cos(2\pi/25))$  harmonic filter submodule, and so on to obtain amplitude correction coefficients in the 4th, 6th and 8th filter operators.

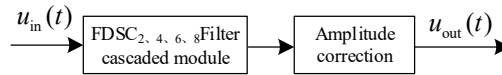


Figure 4. Cascade FDSC Filter Control Diagram

## 5. HC-SVG DC Voltage Control Optimization

### 5.1 Optimization of Interphase DC Voltage Control in CHB

The Self-Describing Filter Tree (SDFT) module in the Cascaded H-Bridge (CHB) converter is substituted with the Filtered-Distributed Switch Capacitor (FDSC) cascade filter operator module to effectively filter harmonic components. This modification optimizes the zero-sequence voltage waveform necessary for preserving inter-phase voltage equilibrium during unbalanced and grid fault scenarios. Consequently, it helps mitigate the imbalance in the inter-phase DC voltage of the CHB module to a significant degree.

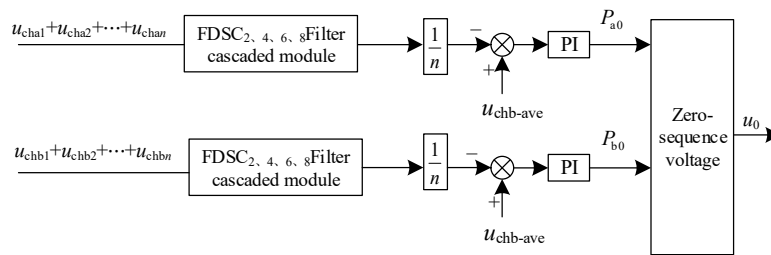


Figure 5. Cascade FDSC Filter Control Diagram

### 5.2 Optimization of DC Voltage Control at NPC Side

As illustrated in Figure 6, an FDSC cascaded filter operator module is inserted prior to feeding the actual DC-side voltage  $u_{dc}$  of the NPC power unit into the PI controller. This module is designed to eliminate harmonic components, thereby achieving control optimization.

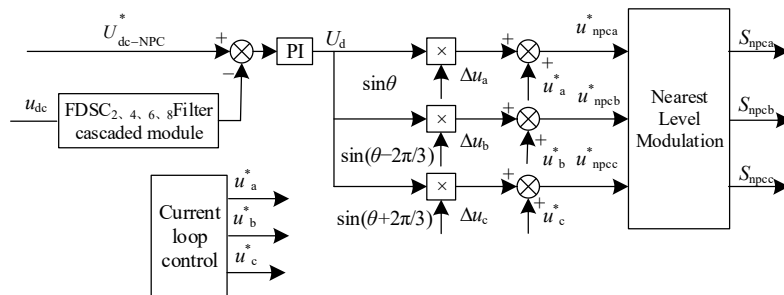


Figure 6. Optimization of DC Voltage Control for NPC Power Units

## 6. Simulation

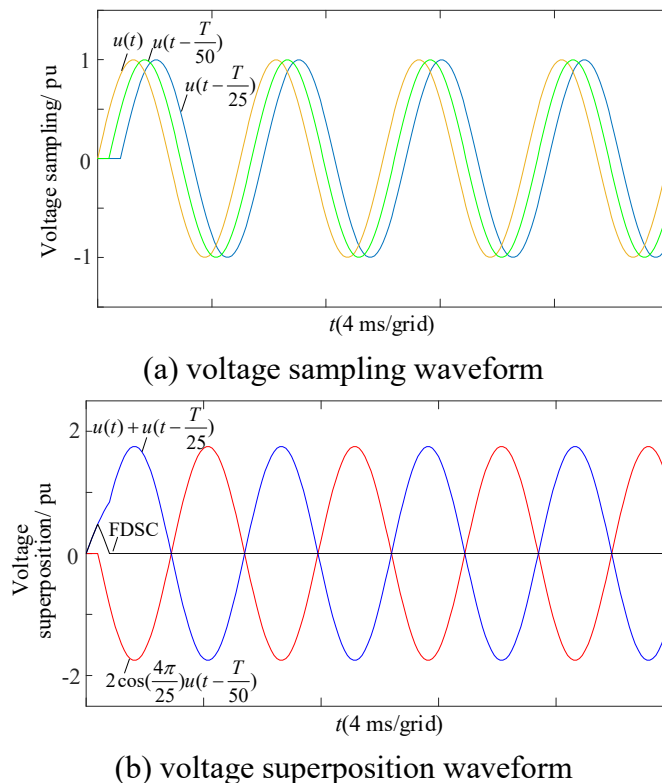
The 6kV/3Mvar three-phase HC-SVG proposed in this study is simulated and validated using the Matlab/Simulink simulation platform. Simulation parameters are detailed in Table 1, including a DC side capacitance of 15000 $\mu$ F for the NPC three-level power unit and 500 $\mu$ F for the sub-module of the CHB power unit.

**Table 1.** Main circuit parameters

Parameters	Topology
Effective value of line voltage $U_s$ /kV	6kV
Compensation capacity $Q$ /Mvar	3Mvar
The peak value of rated compensation current	408A
Equivalent inductance value of filtering reactor $L$ /mH	3.05mH
The DC-side voltage command value of the NPC power unit	7.053 kV
The DC-side voltage command value of the CHB power unit	2130V
Number of CHB submodules	3

### 1) Principle simulation of delay-cancellation filtering.

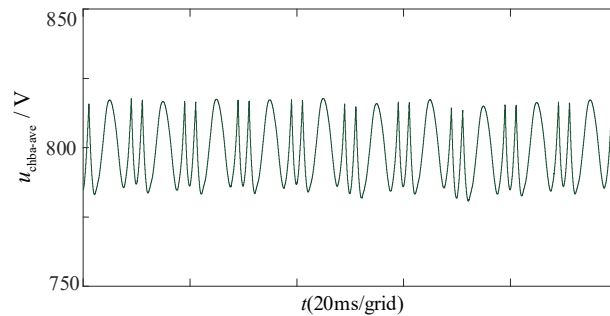
The delay cancellation filter is implemented using Matlab simulation, and its effectiveness is confirmed through the configuration of predetermined parameters. The time-domain waveform of  $h=4$  harmonics post FDSC( $2\cos(4\pi/25)$ , 50) third sampling and superposition is depicted in Figure 7. It is evident that the instantaneous values of  $u(t)+u(t-T/25)$  consistently exhibit equal magnitudes but opposite directions to  $u(t-T/50)$ , resulting in complete mutual cancellation.



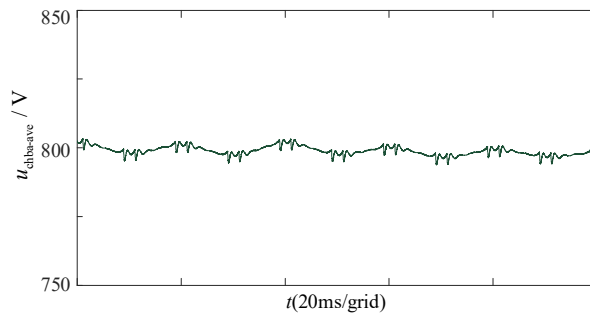
**Figure 7.** Time domain diagram of  $h=4$ th harmonic filtered by FDSC( $2\cos(4\pi/25)$ , 50)

2) Simulation analysis of improved dc side control method based on delay cancellation method.

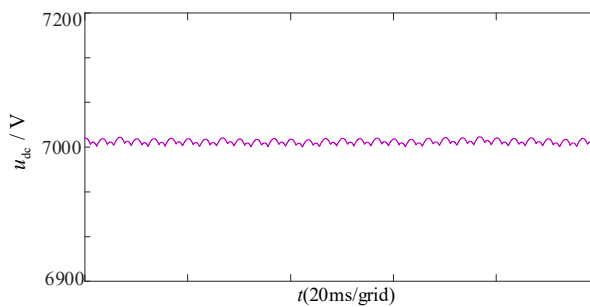
Assuming HC-SVG operates with an output rated capacitive reactive power of 3 Mvar, a simulation comparison was conducted using the original DC side control method and an optimized DC side control method. Figures 8(a) and (c) display the average capacitance voltage waveform of phase A DC side of the CHB unit and the capacitance voltage waveform of the NPC unit under the original control scheme. Figures 8(b) and (d) show the DC voltage waveforms under the optimized control scheme. The simulation results clearly indicate that the output voltage waveform of both the CHB unit and NPC unit are optimized, and the DC voltage of each component is more stable with the addition of the FDSC cascade operator.



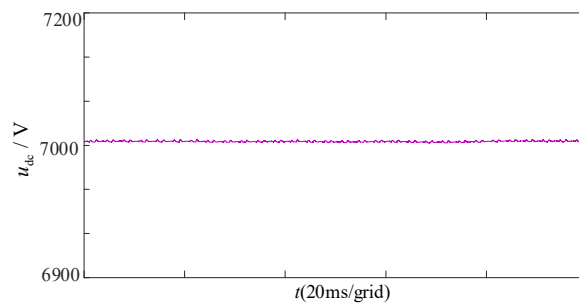
(a) Average capacitance voltage waveform of phase A DC side of CHB unit



(b) Average capacitance voltage waveform at DC side of phase A of CHB unit after filtering



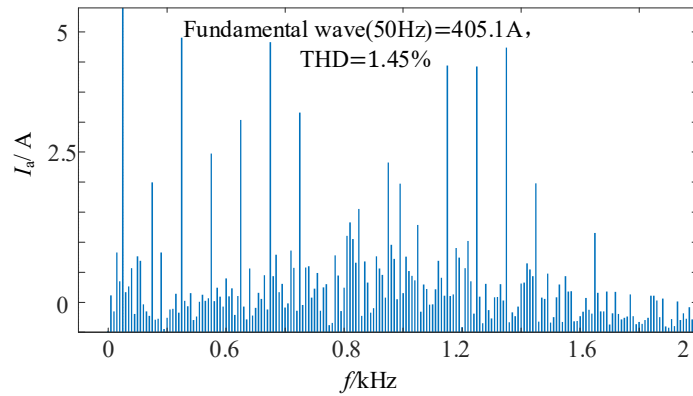
(c) DC side capacitance voltage waveform of NPC unit



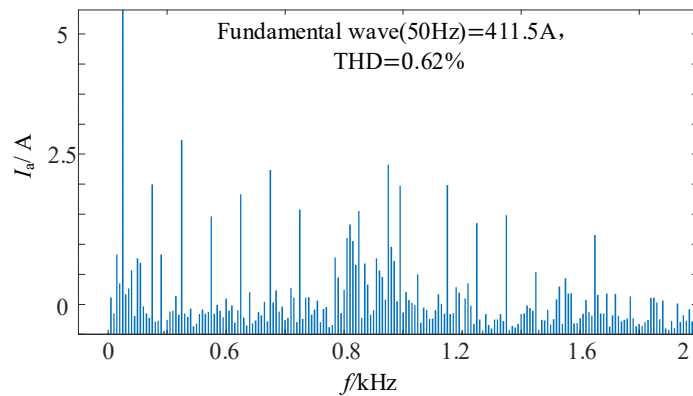
(d) Filtered NPC unit capacitance voltage waveform

**Figure 8.** Comparison of voltage waveforms before and after adding FDSC filtering

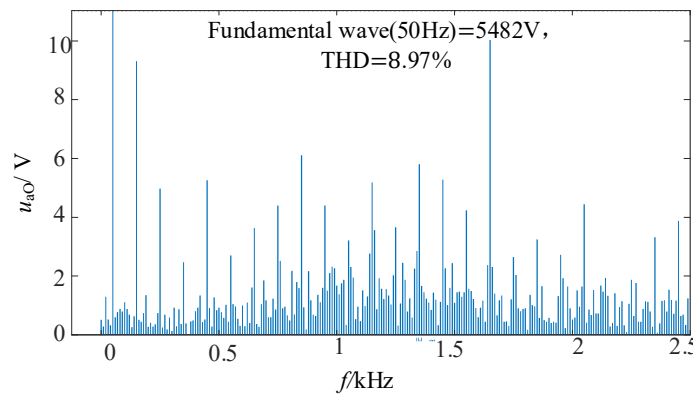
Figure 9 depicts a harmonic analysis of phase A output current and voltage in HC-SVG. Simulation results indicate that implementing a delay signal cancellation filtering method based on the vector triangle principle enhances the total harmonic distortion (THD) of HC-SVG output voltage and output compensation current under identical operating conditions, thereby improving the compensation characteristics of HC-SVG. During power grid faults with significant negative sequence voltage, the inter-phase balance control of CHB relies heavily on the equilibrium of CHB capacitor voltage. Optimizing the control strategy in this context can further ensure the stable operation of HC-SVG during fault conditions.



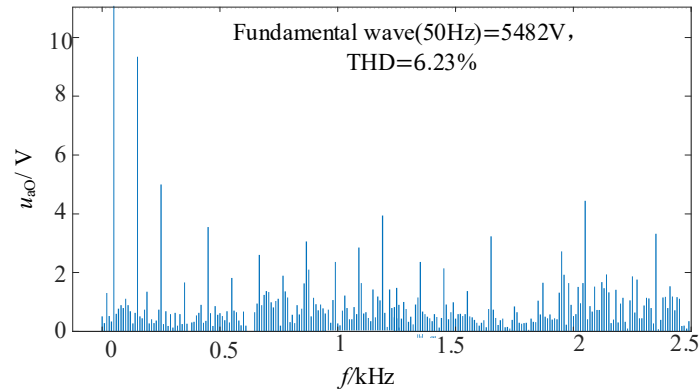
(a) Output phase voltage  $I_a$  harmonic analysis waveform



(b) Harmonic analysis waveform of filtered output phase voltage  $I_a$



(c) Output phase voltage  $u_{aO}$  harmonic analysis waveform



(d) Harmonic analysis waveform of output phase voltage  $u_{aO}$  after filtering

**Figure 9.** Comparison of voltage waveforms before and after adding FDSC filtering

## 7. Conclusion

(1) To address the issue of excessive harmonic components in the DC side capacitor voltage of HC-SVG impacting the precision of the DC side voltage balance control loop, we analyze the harmonic characteristics of the DC side capacitor voltage through theoretical examination of CHB and NPC unit modulation voltages. We introduce a delay signal cancellation filtering technique grounded in the vector triangle principle to enhance DC side voltage control optimization.

(2) The optimization control strategy proposed enhances the compensation performance of HC-SVG. Simulation results demonstrate an enhancement in the total harmonic distortion (THD) of both the output voltage and compensation current of HC-SVG under identical operating conditions, thereby improving the compensation characteristics of HC-SVG.

## References

- [1] Du Shaotong, Liu Jie, Zhou Juan, et al. A 6kV Static Var Generator Based on NPC and H Bridge Hybrid Cascade [J].2021-10-14.
- [2] Du Shaotong, Tan Xingguo, Zhou Juan. Capacitance value analysis and DC voltage control of H-bridge cascade STATCOM with reduced capacitance [J]. Power Grid Technology, 2019, 43 (1): 275 - 284.
- [3] Nan Yannan, Lu Xiangdong. Research on SVG power reactive power compensation based on filter lifting [J]. Grid and Clean Energy, 2018, 34 (5): 31-35.
- [4] Liu Y ,Guo Z ,Liu F , et al.A Real-Time Diagnosis Method of Open-Circuit Faults in Cascaded H-Bridge RectifiersBasedonVoltage Threshold and Current Coefficient of Variation[J].Electronics,2025,14(5):986-986.
- [5] Li Xinian, Xu Tao, Niu Decun. Fast Delay Signal Cancellation Filtering Method Based on Vector Triangle Principle [J]. Journal of China Electrical Engineering, December 5, 2021.
- [6] Yang Shaobo, Zeng Siming, Zhou Wen, et al. Delay signal phase lock cancellation technology and analysis of delay error effect [J]. Power Electronics Technology, 2021, 55(09): 31-35+47.