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A Review of the Impact of Dead-time Control on Switching Device Efficiency Analysis and Optimisation Strategies

Xiang Li*

Department of Electric and Electronic Engineering, University of Liverpool, Brownlow Hill,
Liverpool, L69 3BX, United Kingdom

*Corresponding author's e-mail: sgxli79@liverpool.ac.uk

Abstract

Dead time is a key factor affecting the efficiency and reliability of power electronic systems, especially in switching devices such as MOSFETs and IGBTs. In this paper, we systematically review the mechanism of dead time control on switching loss, conduction loss and overall system performance, and discuss the optimisation strategies. The study aims to integrate the existing results, analyse the key technical challenges, and provide efficiency improvement solutions for motor drive and new energy applications. In this paper, we firstly define the concept of dead time and its important role in some circuit models in order to prevent short-circuiting, and then analyse its correlation characteristics with power loss and voltage distortion. The scope of the review covers traditional silicon-based devices and new wide-band semiconductors (SiC/GaN), comparing the efficiency, complexity, and so on, of deadband control under different models.

Keywords

Deadband Control; Switching Losses; Power Electronics; Optimisation Strategies; Wide-Bandwidth Devices; Adaptive Control.

1. Introduction

The efficiency optimisation of power electronic converters has been the focus of research in both industry and academia, in which the precise control of the dead time has a decisive impact on the loss of the switching devices, the quality of the output waveforms and the reliability of the system. In bridge circuits, although the introduction of dead time can avoid the short-circuiting of the upper and lower tubes, the excessively long dead time will lead to voltage distortion and increased conduction loss, while the excessively short dead time may lead to safety hazards.

Conventional fixed deadband control enforces the need to wait a fixed delay before switching on another pair of tubes after either switch is turned off by inserting a preset delay time (Tdead) between the upper and lower tube drive signals [1]. Although the fixed deadband is simple to implement, this method causes waveform distortion due to attenuation of the fundamental amplitude of the output voltage and low harmonic distortion [2]. More grimly, the prevalence of wide-bandwidth devices (SiC/GaN) exacerbates the contradiction - their switching speeds are on the order of nanoseconds, and the time-dependent ratio of the fixed deadband (Tdead/Ts) expands dramatically at high frequencies.

With the demand of higher power converters, the switching frequency will be increased several times [1]. Therefore, the dead-time optimisation problem in high-frequency switching scenarios is further highlighted, and the traditional fixed deadband strategy is no longer able to meet the demand for high efficiency. In recent years, a number of models and techniques have been proposed to improve the demand for high efficiency in dead-time control [1-10]. However, existing methods are still controversial in terms of electromagnetic interference (EMI) and the co-optimisation of dead zones under complex load conditions and the co-optimisation of dead zones. The aim of this paper is to systematically analyse the applicability and limitations of two typical deadband control models (zero-voltage switching and adaptive dead-time control), focusing on the comparison of circuit parameter-based, real-time feedback. The full paper is structured as follows: Section II analyses the dead-time loss mechanism, Section III reviews and compare the mainstream control models, and Section IV summarises the challenges and trends.

2. Principle of Dead-time

2.1 PWM Modulation

PWM is a kind of pulse width modulation, assuming that a digital signal high level is 5V and low level is 0V, then we want to output different analogue voltages, we need to use PWM, by changing the duty cycle of the output square wave so as to obtain an analogue voltage signal simulated with a digital signal. Let’s say the duty cycle is 50%, that is, half the time for high level, half the time for low level, at a certain frequency, you can get an analogue 2.5V output voltage, then 75% of the duty cycle to get the voltage is 3.75V. We can understand this principle more intuitively in Figure 1. The regulating effect of pwm comes from the control of the width of the ‘duty cycle’, the ‘duty cycle’ becomes wider, the output energy will be increased, and the average voltage value obtained through the resistive converter circuit will rise, the ‘duty cycle’ becomes narrower, the average voltage value of the output voltage signal will be reduced, and the average voltage value obtained through the resistive converter circuit will fall. If the ‘duty cycle’ is narrower, the average value of the output voltage signal will be reduced, and the average voltage value obtained by the resistor-converter circuit will also be reduced That is to say, under a certain frequency, different output analogue voltages can be obtained through different duty cycles.

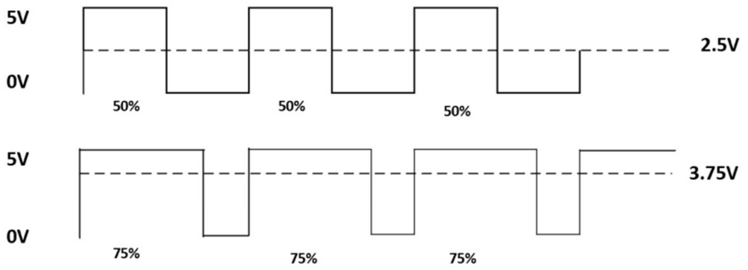

Figure 1. PWM mechanism

2.2 Dead Time

So the dead time is the PWM output, in order to make the full-bridge or half-bridge of the upper and lower tubes will not occur because of the switching speed of the problem of simultaneous conduction and set up a protection time. So in this time, the upper and lower tubes will not have output, of course, the waveform output will be interrupted, the dead time is generally only a few percent of the cycle.

3. Two Typical Deadband Control Models

3.1 Zero Voltage Switch(ZVS)

In conventional hard-switching circuits, the switching devices operate at non-zero voltages/currents, resulting in switching losses, and this loss relationship can be seen in Equation (1).

$$Psw \propto V \cdot I \cdot fsw \qquad (1)$$

Zero Voltage Switching (ZVS) significantly reduces switching losses by ensuring that the voltage across the switching tube is zero at the moment of conduction, eliminating voltage-current overlap. It mainly relies on a zero-voltage mechanism, i.e., the use of resonant or inductive currents to discharge the junction capacitance of the switching tube, which reduces VDS to zero.

We will use a half-bridge LC resonant circuit in Fig. 2 to specify the operation of the ZVS.It is divided into four main operating times (start-up time, t0~t1 time, t1~t2 time and t2 time). In Fig. 2(a) we see the complete ZVS circuit structure, which is a switching part consisting of two mos-tubes (one pmos and one nmos), as well as a capacitive-inductive LC resonant part, and a half-bridge circuit consisting of some diodes and resistors. In the start-up process, at the beginning of the power supply L1 passes into the current is zero, the power supply through R1, R2 make Q1, Q2 conductive, L1 current gradually increased. Due to the two switching tube characteristics (Q1 is nmos, Q2 is pmos) differences, will lead to different currents flowing into the two switching tubes, assuming that IQ1>IQ2, so the Q1 gate voltage is higher than the Q2 gate voltage, through the two diodes D1, D2, so that the voltage of the a point is lower than the voltage of the c point, so solenoids T1 will produce a b for positive, a for the negative inductance voltage, and so through the formation of the T1 Positive feedback, so that Q1 conduction, Q2 cut-off. At this time, ZVS complete the start-up process. After completing the start-up process switching tube Q1 conducts and Q2 cuts off. During t0~t1 in Fig. 2(b). Steady state Q1 conduction, because the last cycle T1 current is a to c, and the voltage on both sides of C1 is zero. Since the current cannot be changed abruptly, the T1 current will charge C1, which is gradually a negative c positive voltage and becomes sinusoidally larger, and the T1 current becomes sinusoidally smaller. At this time, the a voltage is pulled down to 0V by Q1, so the voltage at point c becomes sinusoidal, Q1 gate voltage is clamped by the D3 regulator, at this time, the Q1 tube stays on, Q2 is still cut off.

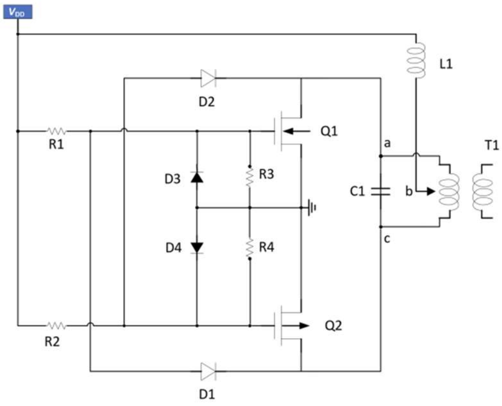

Figure 2. (a) The ZVS circuit of start-up time

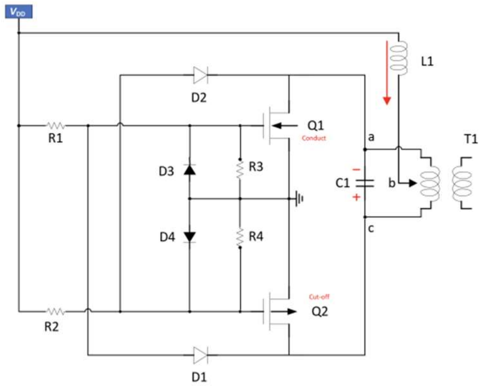

Figure 2. (b) The ZVS circuit of t0~t1 time

At the time of the next mode's phase t1~t2, the charging of capacitor C1 is completed in the previous time phase. At this time, C1 begins to discharge from c to a through T1, the VC1, i.e., the voltage at point c, becomes sinusoidally smaller, and the T1 current becomes sinusoidally larger from c to a. And when VC1 is 0, Q1 truncates and Q2 conducts. To t2 time in Figure 2 (c), when the C1 ability to discharge basically finished, the c point voltage drops to the MOS tube threshold voltage or so, will be through the D2 so that Q1 into the amplification area. At this time C1 on the T1 winding from c to a discharge current reaches its maximum value. At the same time as Q1 into the amplification area, the a point voltage rises gradually, at the same time through D1 to make Q2 also into the amplification area C1 discharge is complete, T1 winding from c to a current reaches its maximum value, will charge C1, so that C1 charging for the a positive and c negative voltage, and at the same time, the voltage at the ends of the C1 sinusoidally large. At this time, the two MOS tubes enter the amplification area at the same time. Due to the continuous charging of T1 on C1, C1 voltage is a positive c negative, through the two diodes so that the Q2 gate voltage increases, Q1 gate gradually decline, while the formation of positive feedback, Q2 conduction (process and start-up phase Q1 conduction mechanism is similar), Q1 cut-off. So, this zvs model performs deadband control of two switching tubes Q1 and Q2 through the above process. Eventually, an oscillating current in Figure 3 is formed in the end. During the process, the L1 inductance value is larger than T1, and the L1 current is basically unchanged throughout the oscillation cycle. The L1 inductance is larger than T1, and the L1 current is basically constant throughout the oscillation cycle.

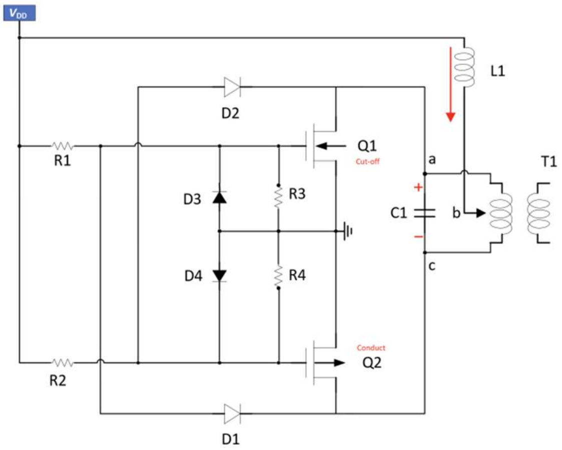

Figure 2. (c) The ZVS circuit of t2 time

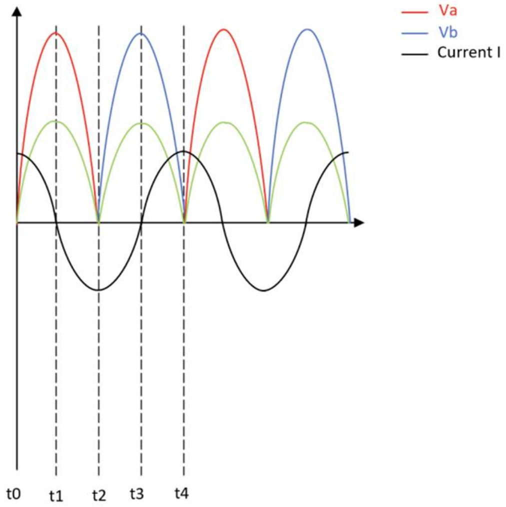

Figure 3. Waveforms of current and voltage in zvs circuit

As can be seen in the basic ZVS circuit above, coupled inductors are used here to implement the zero voltage function [4]. Although the circuit is simple to construct here, still the switching losses do not meet our needs and the boost diode is subject to rapid voltage oscillations. Another way to achieve ZVS functionality is through an auxiliary commutation network [5]. However, the auxiliary switches in this network still suffer from hard switching problems leading to high power consumption.

3.2 Adaptive Dead-time Control

Kim et al showed that the use of an adaptive deadband regulation strategy can significantly improve the operational stability of the system compared to a fixed deadband control scheme.As in the previous analyses for ZVS, we also cut from the power consumption equation Equation (2) [9]. An excessively long deadband leads to an increase in diode renewal time, generating additional conduction losses as well as causing problems such as output voltage/current distortion. And insufficient deadband may trigger a straight-through short circuit.

$$\mathrm{Ploss} = \mathrm{VF} \cdot \mathrm{I} \cdot \mathrm{Tdead}/\mathrm{Ts} \tag{2}$$

Therefore, in adaptive dead-time control in Fig. 4, the deadband time can be dynamically adjusted by detecting the circuit state in real time and adjusting the deadband time.

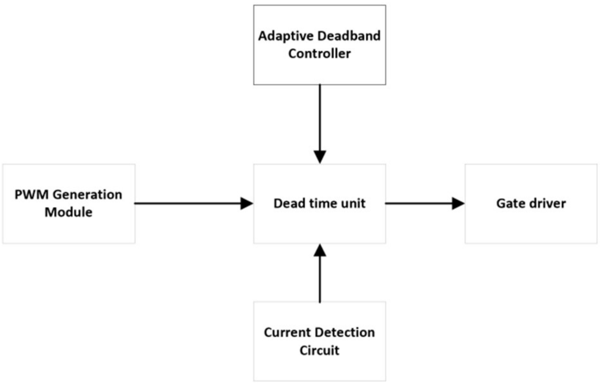

Figure 4. Adaptive Deadband Control Module

The core idea of adaptive deadband control is to dynamically adjust the dead-time Td (related to the load current Iload, bus voltage Vbus, etc.) through real-time feedback of the circuit state, so that it is always within a safe and efficient range. In Figure.4, PWM generation module, as we discussed in section 2. The PWM generation module acts as a signal source and uses a digital timer (e.g. STM32F334) to generate a high frequency PWM wave with a fixed duty cycle. Its duty cycle resolution directly affects the output accuracy, Provideing reference timing for subsequent deadband adjustments [6]. The module outputs the raw PWM signal to the dead time insertion unit, whose rising/falling edges will be dynamically delayed in subsequent sessions.

In the architecture of an adaptive control system, the current detector (usually realised as a current sensor or shunt resistor-based detection circuit) assumes the central function of providing critical state feedback. The core principle of operation is the real-time, accurate conversion of the physical quantity of current flowing through the controlled object into a linearly proportional, low-level voltage signal for subsequent processing. This conversion process, through the measurement of series low-value precision shunt resistor (Shunt Resistor) voltage drop across the terminals (following Ohm's law $V = I \cdot R$) and high common mode rejection ratio of the differential amplifier conditioning, the essence is to achieve high-fidelity conversion of current to voltage. The voltage signal is then digitised by a high-speed analogue-to-digital converter (ADC) and read by the core controller (e.g. MCU, DSP). According to the current detection architecture proposed by Ma et al, when the compensation current is set to 2.6 μA, the structure is able to achieve a stable peak current detection of up to 3.9 A, which exhibits excellent detection accuracy and stability [7].

Adaptive Control Circuit (Adaptive Control Circuit) is a kind of intelligent control structure that can automatically adjust the control parameters according to the dynamic changes of the system, and its core objective is to maintain the optimal control performance in the case of unknown or time-varying system parameters. The key to Adaptive Control Circuit lies in its dynamic adjustment capability, which is commonly used in the circuit to adaptively control the phase current directly or indirectly. Chen et al [8] designed two on-chip buck converters with 5V input and 1.2V/1A output using conventional control and current-mode adaptive conduction control, respectively. The experimental results show that the adaptive conduction control scheme has significant advantages in performance.

3.3 Results and Comparisons

In terms of operating principle, the ZVS is mainly designed to force the voltage across the switching tube to zero before conduction by means of a resonant circuit. Eliminate the overlapping loss of current and voltage of switching transient. The adaptive deadband, on the other hand, dynamically adjusts the deadband time Td, and calculates the optimal deadband by detecting the current polarity or voltage over zero in real time. In terms of loss reduction, zvs mainly eliminates switching losses (in high frequency environments), which can be improved by 5-10% [3]. For adaptive deadband, reducing conduction losses (dominant at low and medium frequencies) can be improved by 2-5% [10]. Adaptive deadband systems have better performance in terms of circuit complexity. For ZVS its high circuit complexity is mainly due to the need for accurate design of resonant parameters (e.g., values of L, C), which represents more cost. Whereas adaptive deadband has a moderate complexity compared to ZVS, which mainly depends on detection sensors and real-time algorithms. Therefore, ZVS has a higher hardware design threshold, while adaptive dead zones are more demanding on software algorithms. In the future, with the discovery and research of new materials and the accompanying optimisation of algorithms. A control system combining ZVS and adaptive control system can be realised to achieve a dead zone control system with lower cost and better efficiency. A brief comparison between ZVS and Adaptive Deadband in terms of principle, power consumption, complexity, and future prospects can be seen in Table 1.

Table 1. The comparision of the ZVS and Adaptive Dead-Time Control

	Zero Voltage Switching (ZVS)	Adaptive Dead-Time Control
Basic Principle	Achieves switching at V=0 by resonant energy transfer	Dynamically adjusts dead-time to minimize body diode conduction
Efficiency	Over 95% [3]	Around 92% - 95%
Implementation Complexity	Requires precise resonant tank design Sensitive to parasitics	Needs fast current sensing Requires real-time processing
Future Development	AI-assisted resonant tuning	Integrated smart drivers Machine learning prediction

4. Conclusion

This paper presents a systematic review of the impact of dead time control on the efficiency of switching devices and optimisation strategies. Dead time is crucial to avoid bridge arm straight-through, but improper settings can significantly increase switching loss, conduction loss, and lead to waveform distortion. The study focuses on two core optimisation models: zero-voltage switching (ZVS) effectively eliminates switching losses (>95% efficiency) by reducing the switching voltage to zero before conduction through the resonance mechanism, which is especially suitable for high-frequency scenarios, but its circuit design is complex and costly; adaptive deadtime control dynamically adjusts the deadtime through real-time detection of the circuit state (e.g., load current, bus voltage) to optimise the on-state losses (92%-95% efficiency). Adaptive deadband control dynamically adjusts the deadband time by detecting the circuit state (such as load current and bus voltage) in real time, mainly optimising the on-state loss (efficiency of 92%-95%), which has obvious advantages in the application of low and medium frequency. Comparative analysis shows that ZVS hardware threshold is high, while adaptive control is more dependent on software algorithms. With the application of new wide-bandwidth devices (SiC/GaN) and algorithm optimisation, a hybrid scheme combining the high efficiency characteristics of ZVS and the flexibility of adaptive control will be the future development direction to achieve a more efficient and lower cost deadband control system.

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